

# JM30\_HR

## DIS/UMA/Muxless Schematics Document

### Sandy Bridge

### Intel PCH

*DY :None Installed*  
*DIS:DIS installed*  
*DIS\_Muxless :BOTH DIS or Muxless installed*  
*DIS\_PX:BOTH DIS or PX installed*  
*DIS\_PX\_Muxless:DIS or PX or Muxless installed.*  
*Muxless: Muxless installed.(PX4.0)*  
*PX:MUX installed.(PX3.0)*  
*PX\_Muxless:BOTH PX or Muxless installed.*  
*UMA:UMA installed*  
*UMA\_Muxless:BOTH UMA or Muxless installed*  
*UMA\_PX\_Muxless:UMA or PX or Muxless installed*

*ANNIE: ONLY FOR ANNIE solution.*  
*PSL: KBC795 PSL circuit for 10mW solution installed.*  
*10mW: External circuit for 10mW solution installed.*  
*65W: for 65W adaptor installed.*  
*90W: for 90W adaptor installed.*

## SM30\_CR CR Block Diagram

**PCB P/N :**

**Revision : -1**

SYSTEM DC/DC APL5916KAI <sup>48</sup>		CPU DC/DC NCP6131S52MNR <sup>42-43</sup>	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0	DCBATOUT	VCC_CORE

SYSTEM DC/DC		45
UP6128PQDD		
INPUTS	OUTPUTS	
DCBATOUT	1D05V_VTT	

<b>SYSTEM DC/DC</b> <b>UP6183PQAG</b>		41
<b>INPUTS</b>		<b>OUTPUTS</b>
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5	

SYSTEM DC/DC		46
UP6165BQKF		
INPUTS	OUTPUTS	
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3	

SYSTEM DC/DC	
NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

<b>VGA</b> <b>RT8208BGQW</b>		92
<b>INPUTS</b>	<b>OUTPUTS</b>	
DCBATOUT	VGA_CORE	

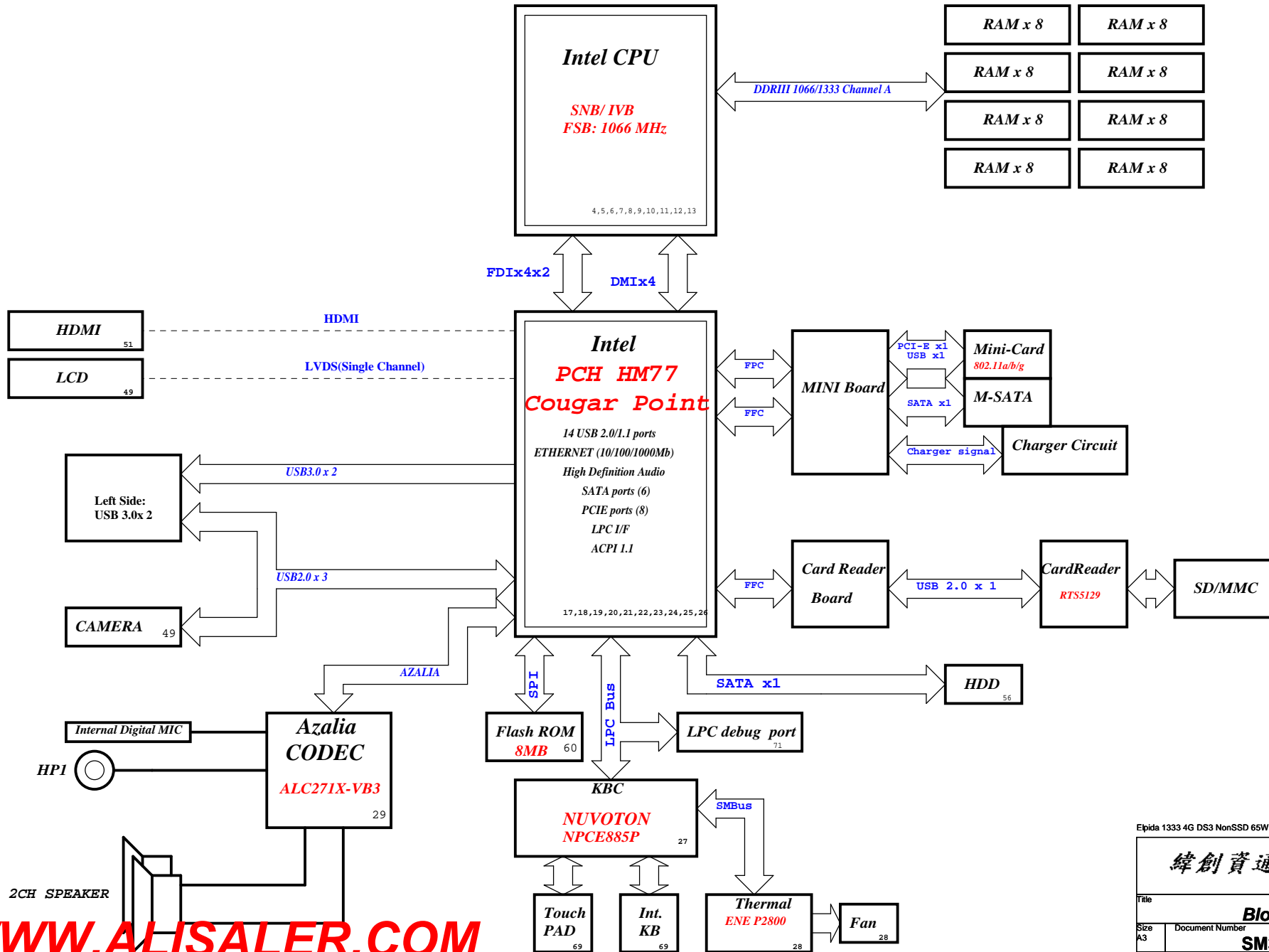
<b>TI CHARGER</b> <b>BQ24745RHDR</b> 40	
<b>INPUTS</b>	<b>OUTPUTS</b>
DCBATOUT	BT+

SYSTEM DC/DC RT9025		47
INPUTS	OUTPUTS	
3D3V_S0	1D8V_S0	

<b>SYSTEM DC/DC</b> <b>RT9025-25PSP</b>		93
<b>INPUTS</b>	<b>OUTPUTS</b>	
1D5V_S3	1V_VGA_S0	
3D3V_S5	1D8V_VGA_S0	

Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

<b>PCB LAYER</b>	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom



Elpida 1333 4G DS3 NonSSD 65W

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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>Block Diagram</b>			
Size A3	Document Number <b>SM30 HR</b>	Rev <b>-SA</b>	
Date: Tuesday, February 21, 2012	Sheet 2 of 102		

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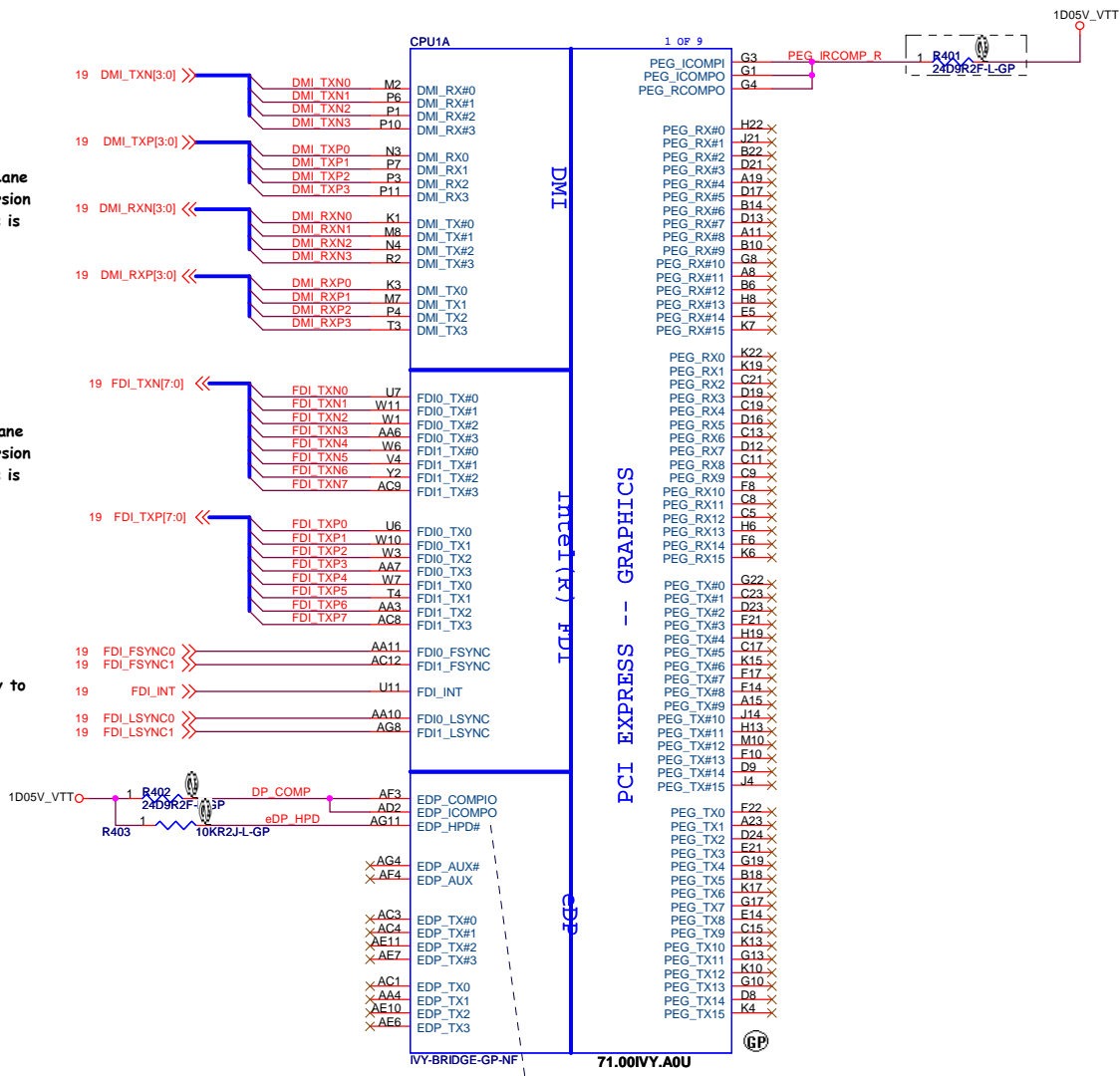


SSID = CPU

Note:  
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:  
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

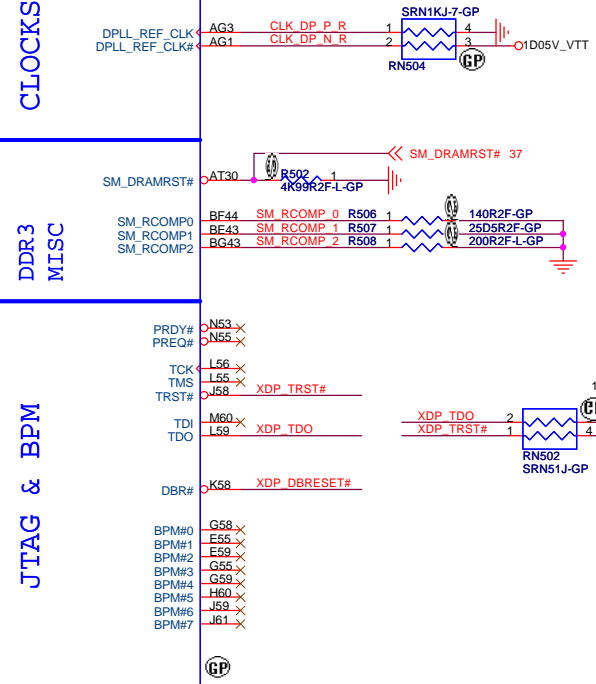
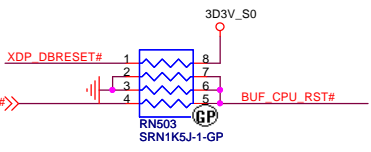
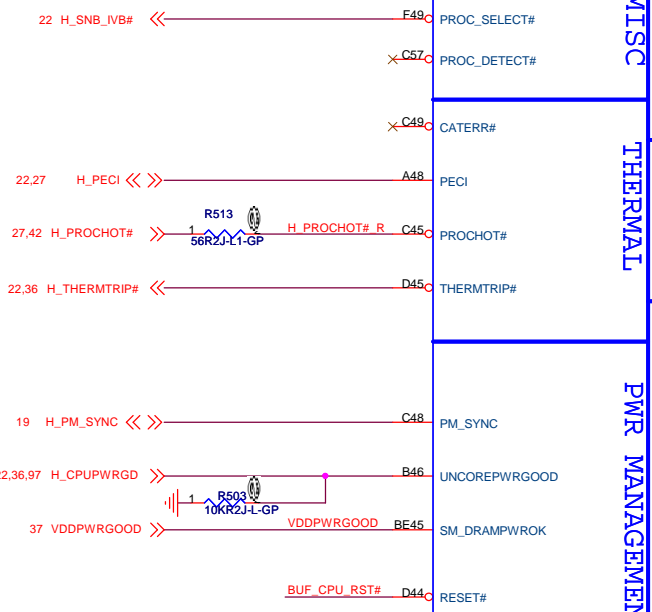
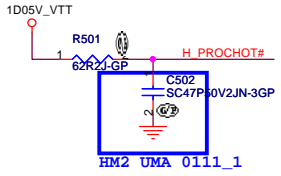
Note:  
Lane reversal does not apply to FDI sideband signals.



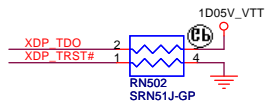
Signal Routing Guideline:  
PEG\_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.  
PEG\_ICOMPI & PEG\_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:  
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

SSID = CPU



Disabling Guidelines:  
If motherboard only supports external graphics or without eDP:  
Connect DPLL\_REF\_SSCLK on Processor to GND through 1K +/- 5% resistor.  
Connect DPLL\_REF\_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.



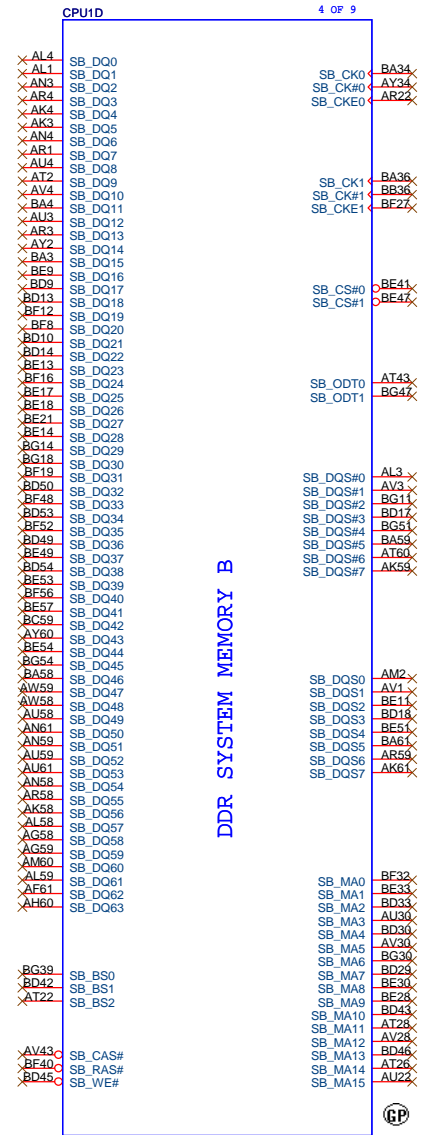
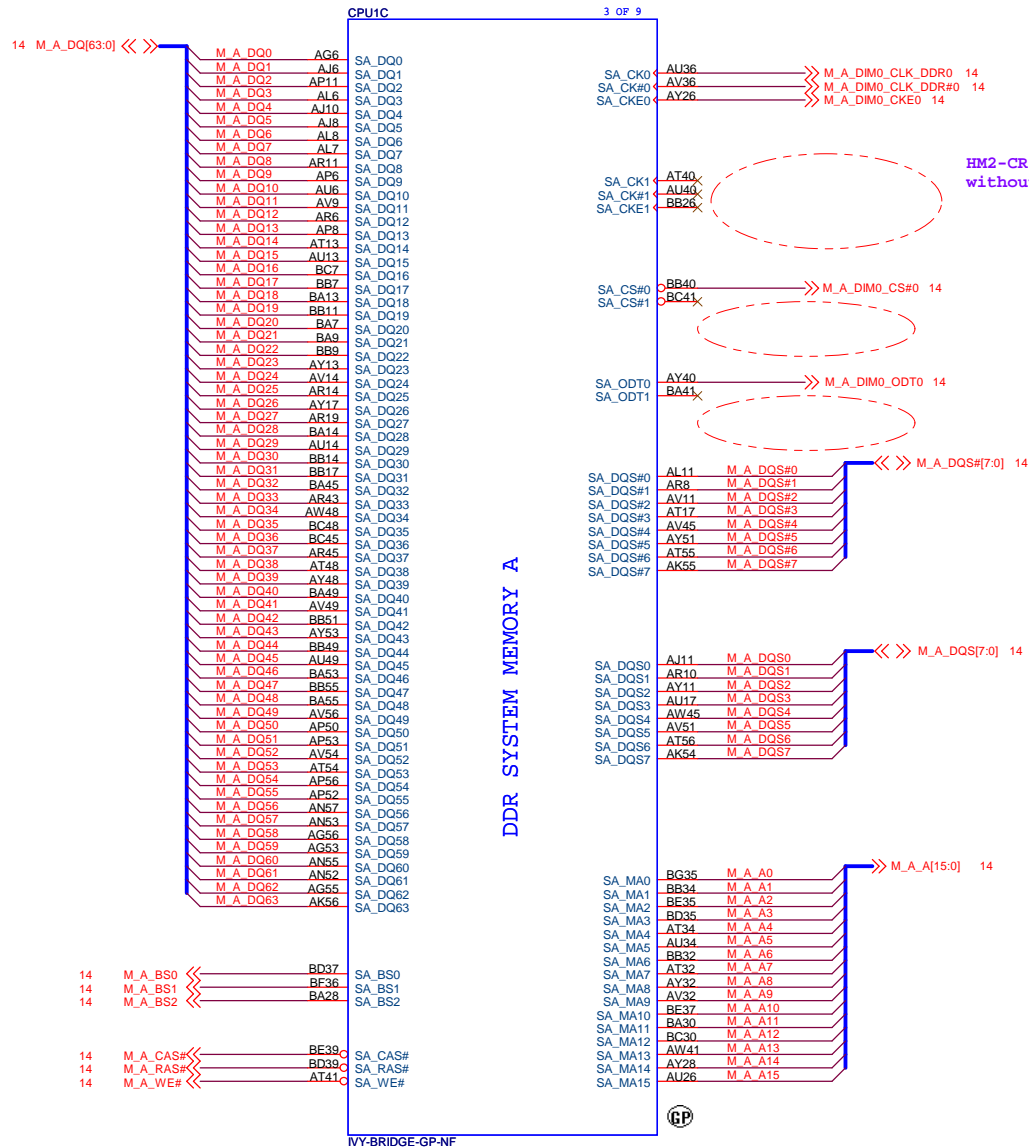
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Title CPU (THERMAL/CLOCK/PM )			
Size A3	Document Number	Rev SA	
Date: Tuesday, February 21, 2012	Rogue	Sheet 5	of 100

SSID = CPU

HM2 UMA 0110\_1



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緯創資通

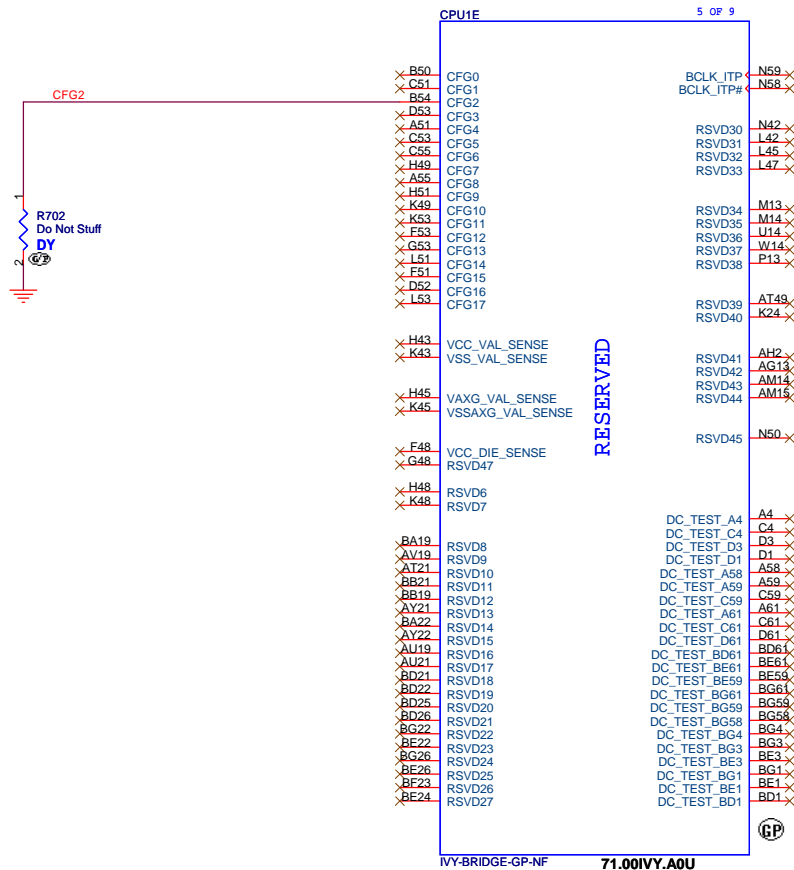
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Taipei Hsien 221, Taiwan, R.O.C.

Title	<i>CPU (DDR)</i>
-------	------------------

Size A3	Document Number <b>Rogue</b>	Rev <b>SA</b>
Date: Tuesday, February 21, 2012	Sheet 6 of	100

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SSID = CPU



Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1 kOhms resistor on the critical CFG[0 trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2]	PCIe Static x16 Lane Numbering Reversal.	1: Normal Operation; Lane # definition matches socket pin map definition  0: Lane Reversed	0
CFG[4]	Display Port Presence strap	1: Disabled - No Physical Display Port attached to Embedded DisplayPort No connect for disable  0: Enabled - An external Display Port device is connected to the Embedded Display Port  Pull-down to GND through a 1KΩ ± 5% resistor to enable port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	00
CFG[17:7]	Reserved configuration lands. A test point may be placed on the board for these lands.		

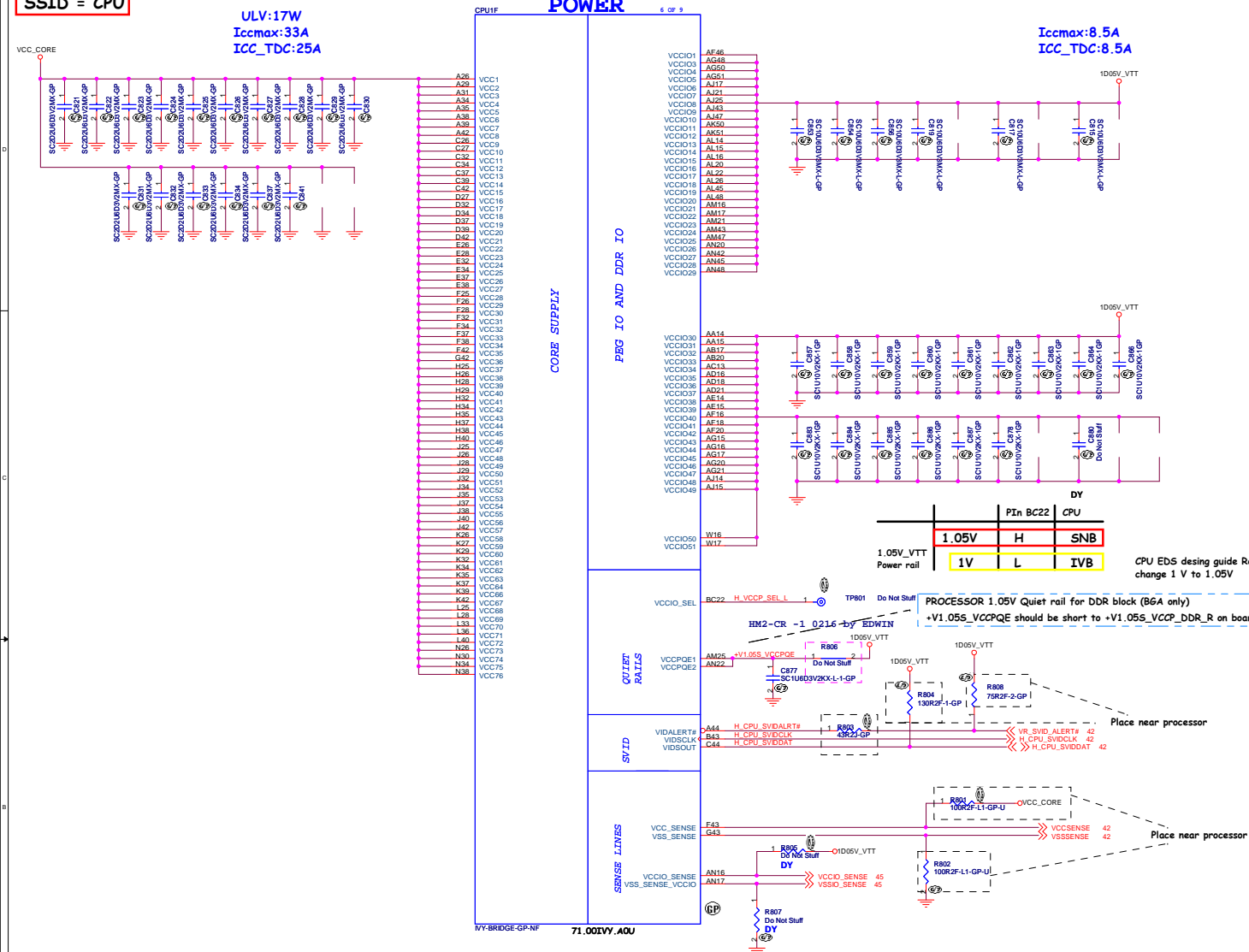
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SSID = CPU

ULV:17W  
Iccmax:33A  
ICC\_TDC:25A

POWER

Iccmax:8.5A  
ICC\_TDC:8.5A



Layout Note: 2.2u Cap place under CPU

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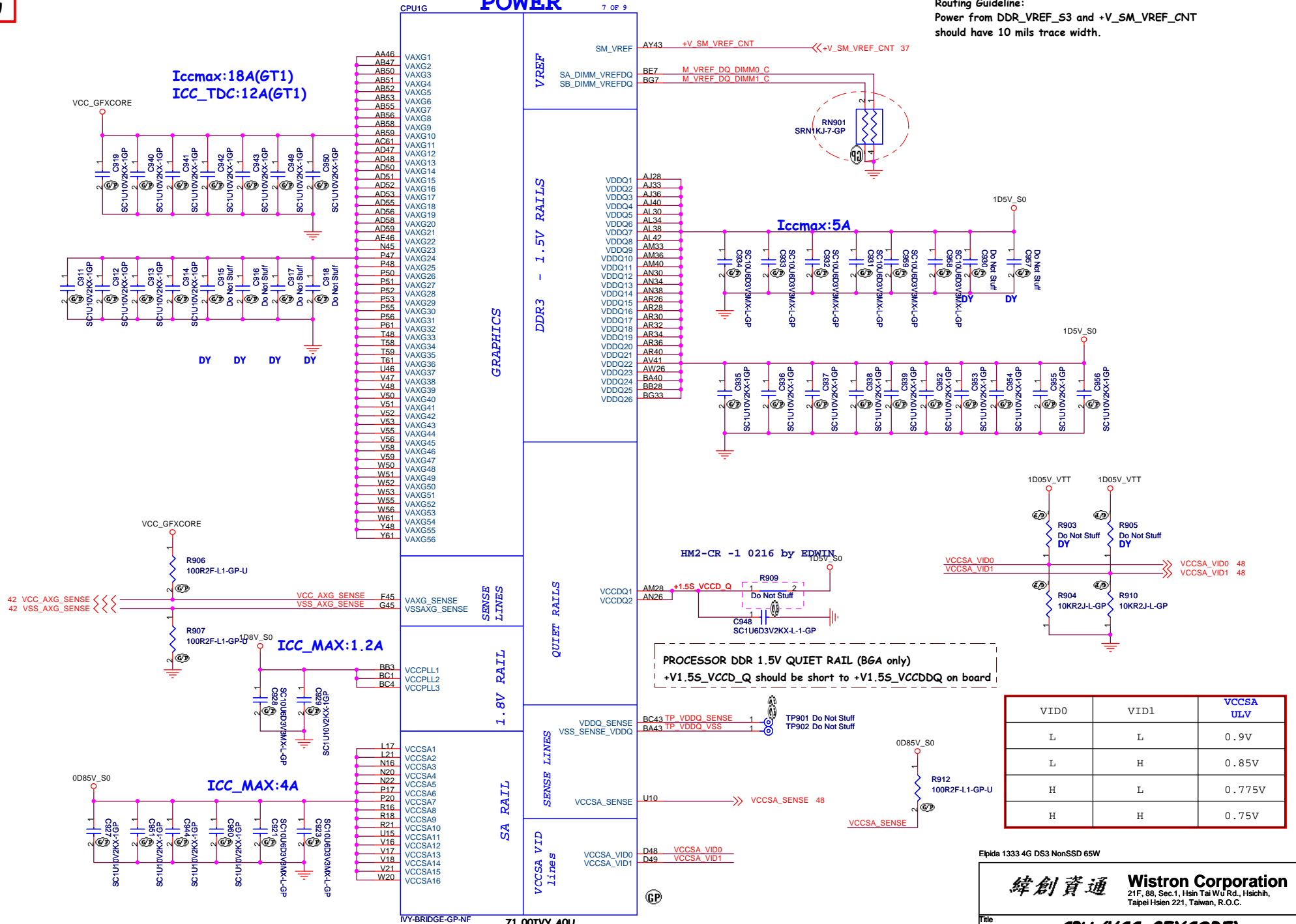
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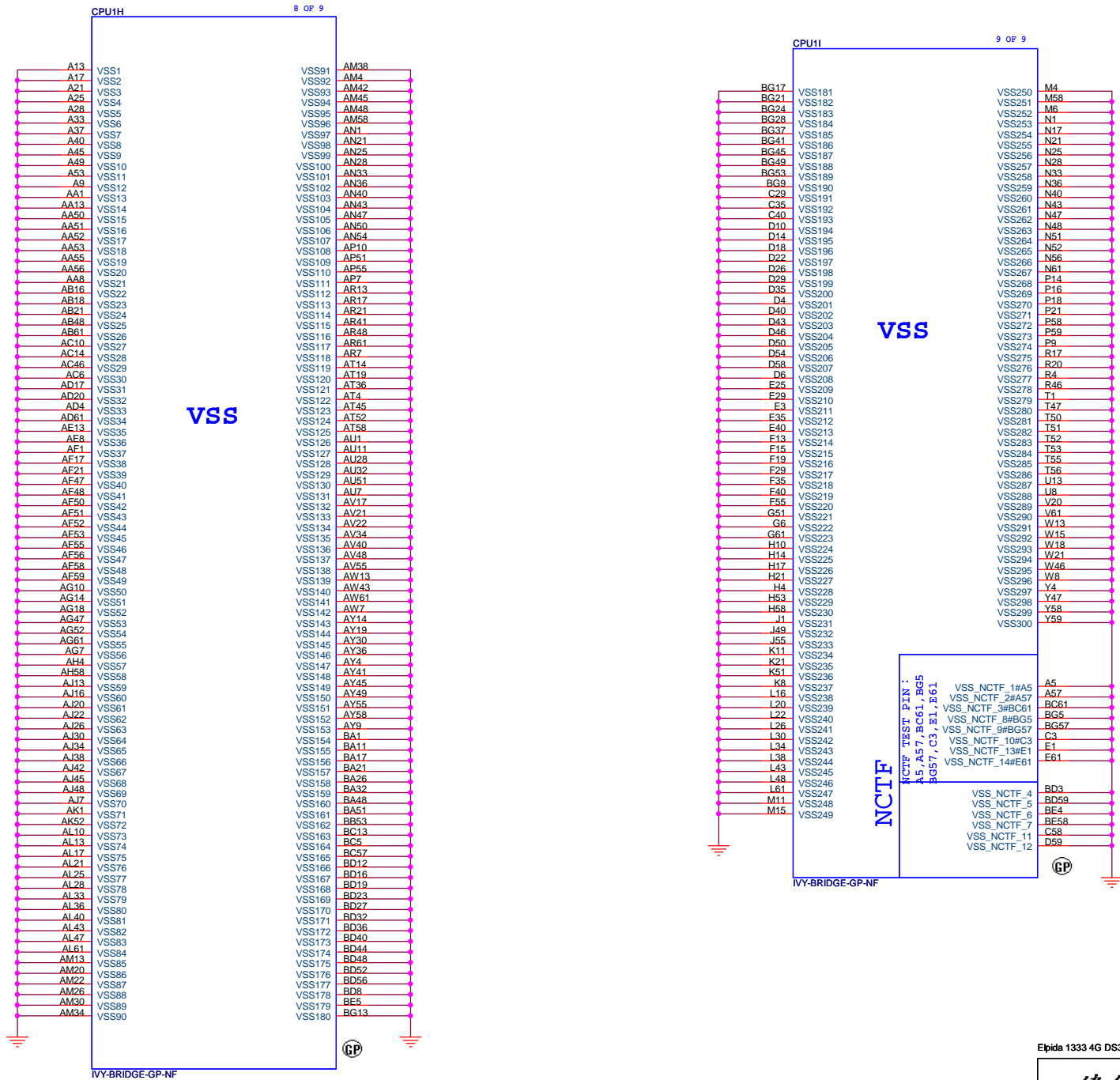
SSID = CPU

## POWER

Routing Guideline:  
Power from DDR\_VREF\_S3 and +V\_SM\_VREF\_CNT  
should have 10 mils trace width.



SSID = CPU



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Blanking

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Title <div>XDP</div>		
Size <div>A4</div>	Document Number <div>SM30 HS</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>11</div> of <div>102</div>

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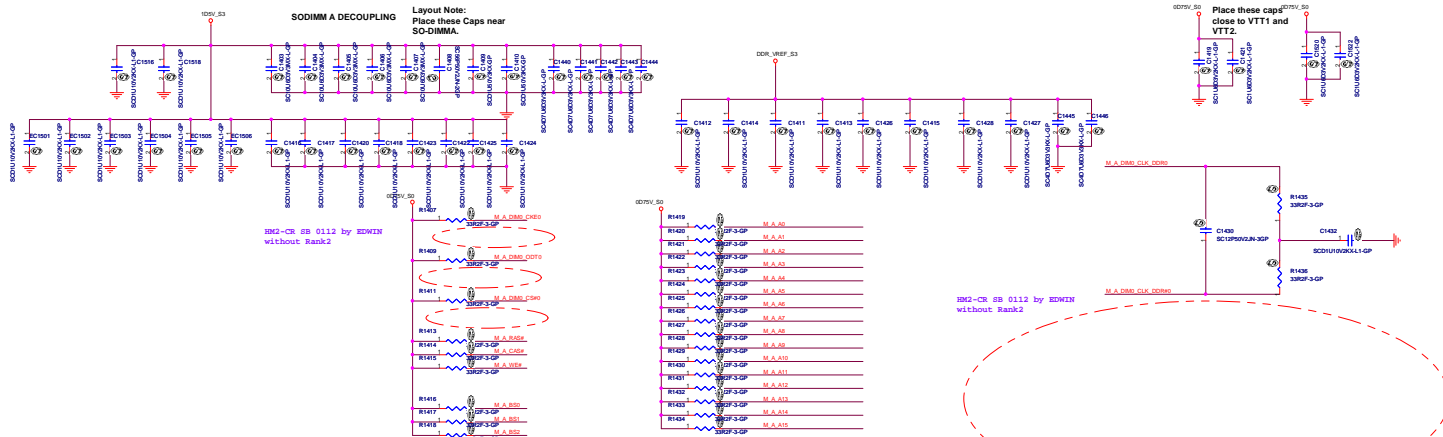
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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>HMA40 HR</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>12</div> of <div>102</div>

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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>SM30 HS</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>13</div> of <div>102</div>

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SSID = MEMORY

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<div>緯創資通Wistron Corporation21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
TitleDDR3-SODIMM2		
SizeCustom	Document NumberSM30 HS	Rev-SA
Date: Tuesday, February 21, 2012	Sheet 15 of	102

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Title

**DDR3-SODIMM2**

Size  
A4

Document Number

**SM30 HS**

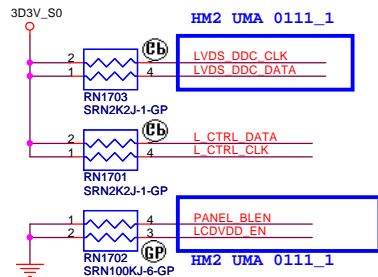
Rev

**-SA**

Date: Tuesday, February 21, 2012

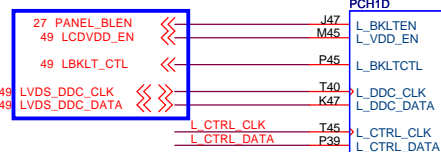
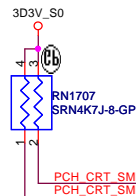
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HM2 UMA 0111\_1

Place near PCH

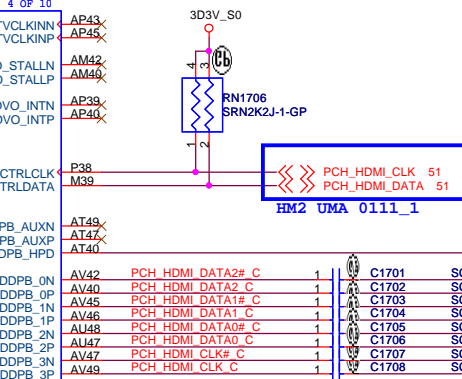


LVDS

Digital Display Interface

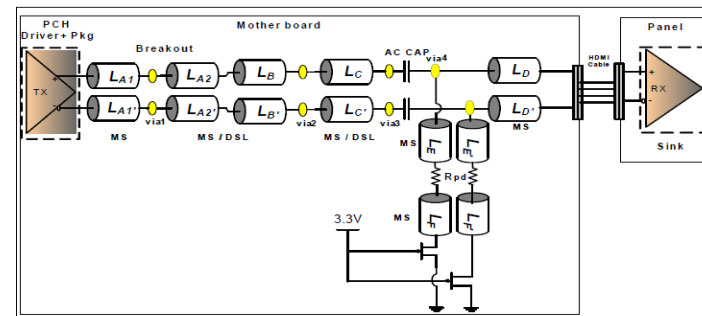
CRT

PANTHER-GP-NF 71.PANTH.00U



Close to Connector side

Impedance:90 ohm TM request to change 85-ohm

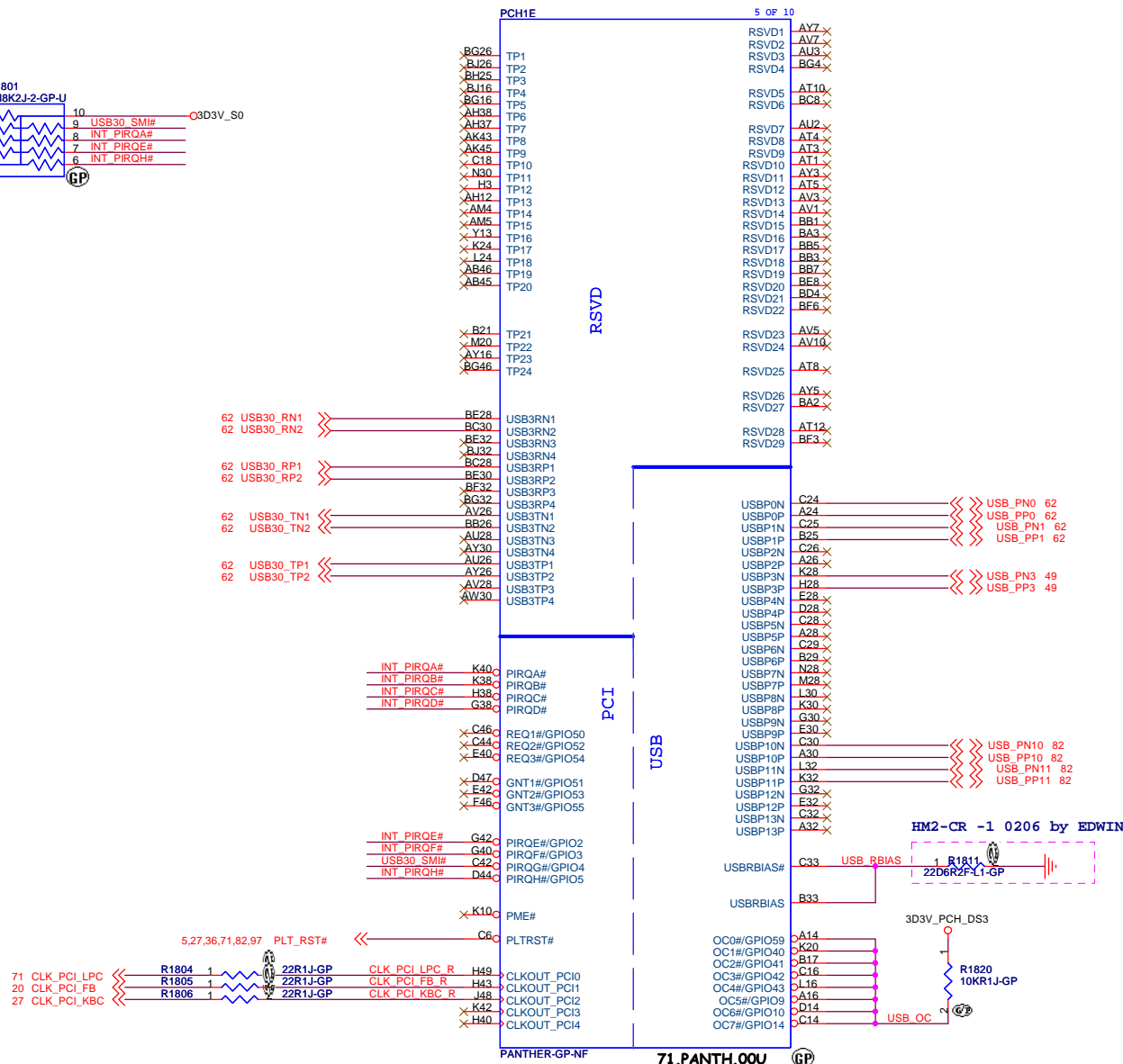
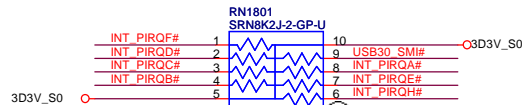


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Title			PCH (LVDS/CRT/DDI)	
Size	Document Number	Rev		SA
A3	SM30-2			
Date:	Tuesday, February 21, 2012	Sheet	17	of 100

SSID = PCH



OC[3:0]# for Device 29 (Ports 0-7)  
OC[7:4]# for Device 26 (Ports 8-13)

USB Table

Pair	Device
0	USB3.0 Ext. port 1
1	USB3.0 Ext. port 2 (Charger)
2	NC
3	BT
4	NC
5	
6	X
7	X
8	
9	
10	Card Reader
11	Mini Card1 (WLAN)
12	CAMERA

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

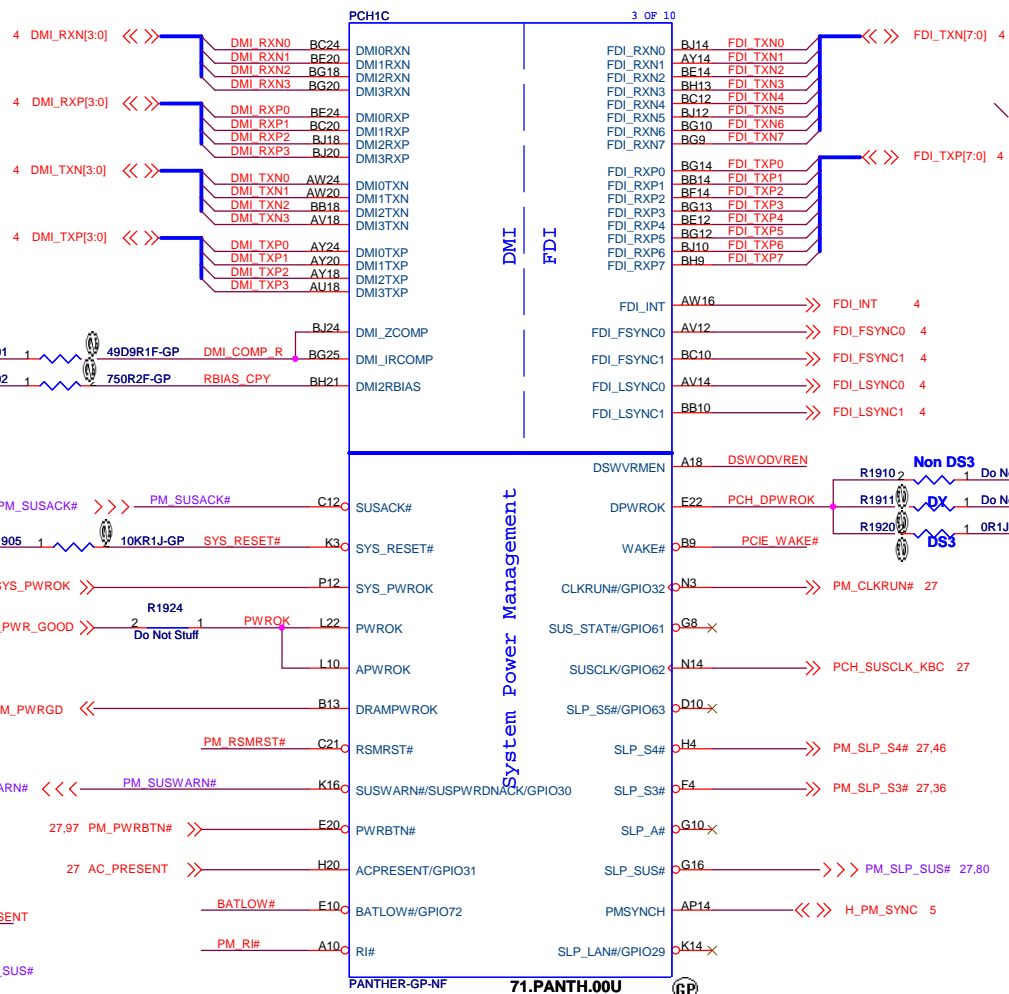
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Title PCH (PCI/USB/NVRAM)			
Size A3	Document Number M41 2SP	Rev SA	
Date: Tuesday, February 21, 2012	Sheet 18	of 100	

SSID = PCH

Signal Routing Guideline:  
DMI\_ZCOMP keep W=4 mils and routing length less than 500 mils.  
DMI\_IRCOMP keep W=4 mils and routing length less than 500 mils.



Deep S4/S5 Supported

Deep S4/S5 Not Supported

VccDSW3\_3

DPWROK

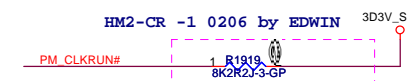
VccSUS3\_3

RSMRST#

For platforms not supporting Deep S4/S5

- 1.VccSUS3\_3 and VccDSW3\_3 will rise at the same time (connected on board)
- 2.DPWROK and RSMRST# will rise at the same time (connected on board)
- 3.SLP\_SUS# and SUSACK# are left as 'no connect'
- 4.SUSWARN# used as SUSPWRDNACK/GPIO30

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



PCIE\_WAKE#  
CRB : 1K  
CEKLT: 10K

PM\_RSMRST#

PM\_SLP\_SUS#

PM\_SLP\_SUS#

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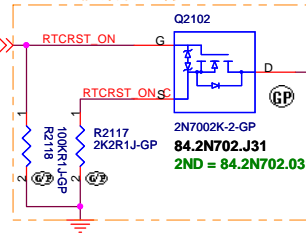
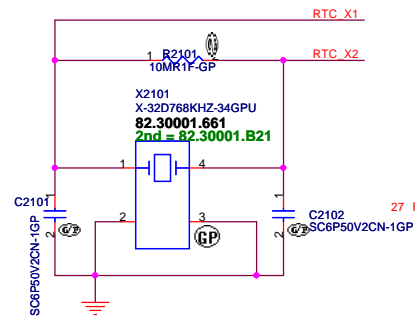
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Title	PCH (DM I/FDI/PM)	
Size A3	Document Number	Rev
	M41 2SP	SA
Date: Tuesday, February 21, 2012	Sheet 19	of 100

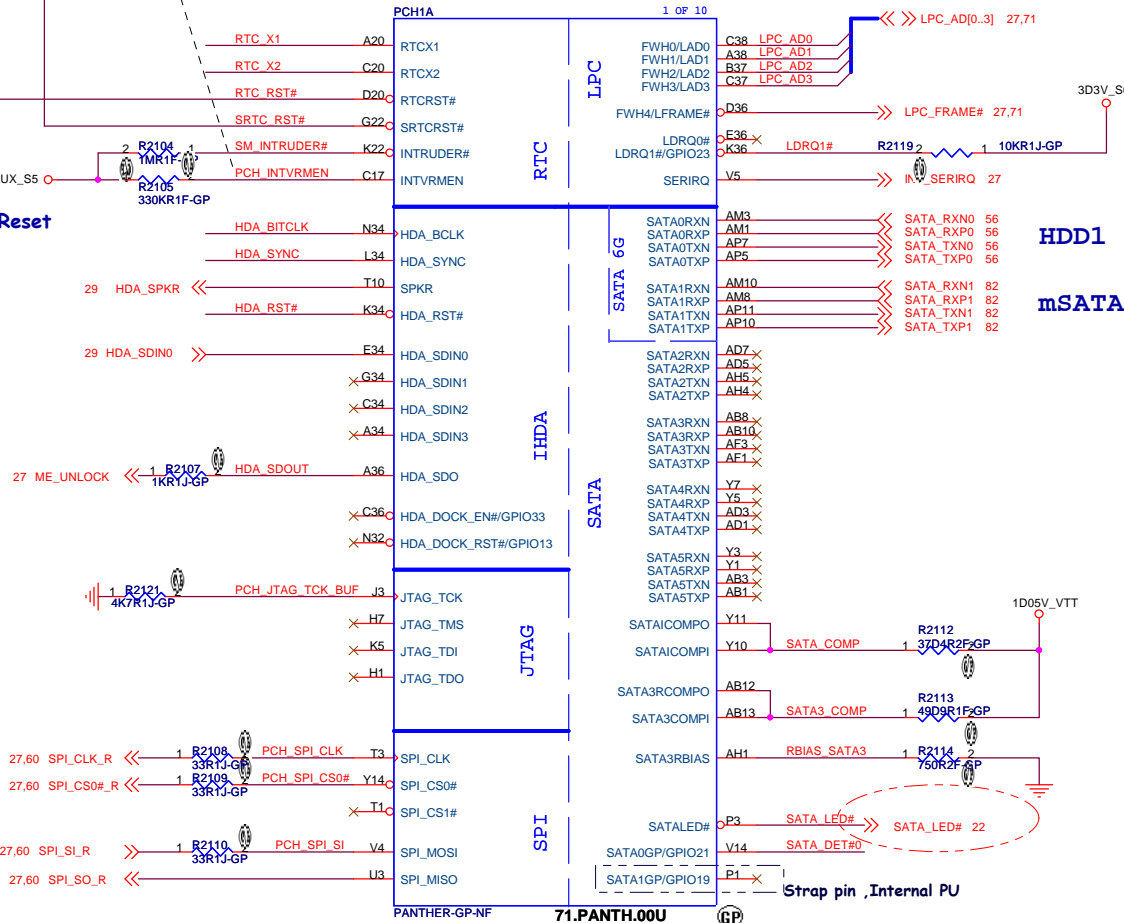
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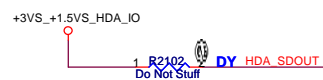
**SSID = PCH**



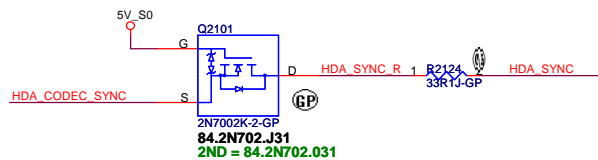
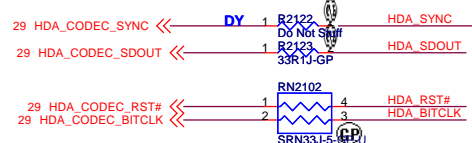
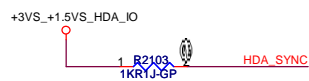
INTVRMEN- Integrated SUS  
1.05V VRM Enable  
High - Enable internal VRs  
Low - Enable external VRs



Flash Descriptor Security Override	
HDA_SDOUT	Low = Default High = Enable

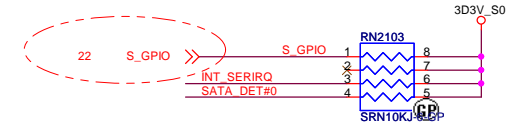


PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V



**HDA\_SYNC:**  
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board.  
Signal may have leakage paths via powered off devices(Audio Codec) and hence contend with the external pull-up.  
A blocking FET is recommended in such a case to isolate HDA\_SYNC from the Audio Codec device until after the Strap sampling is complete.

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HM2-CR SB 0117 by EDWIN  
Swap

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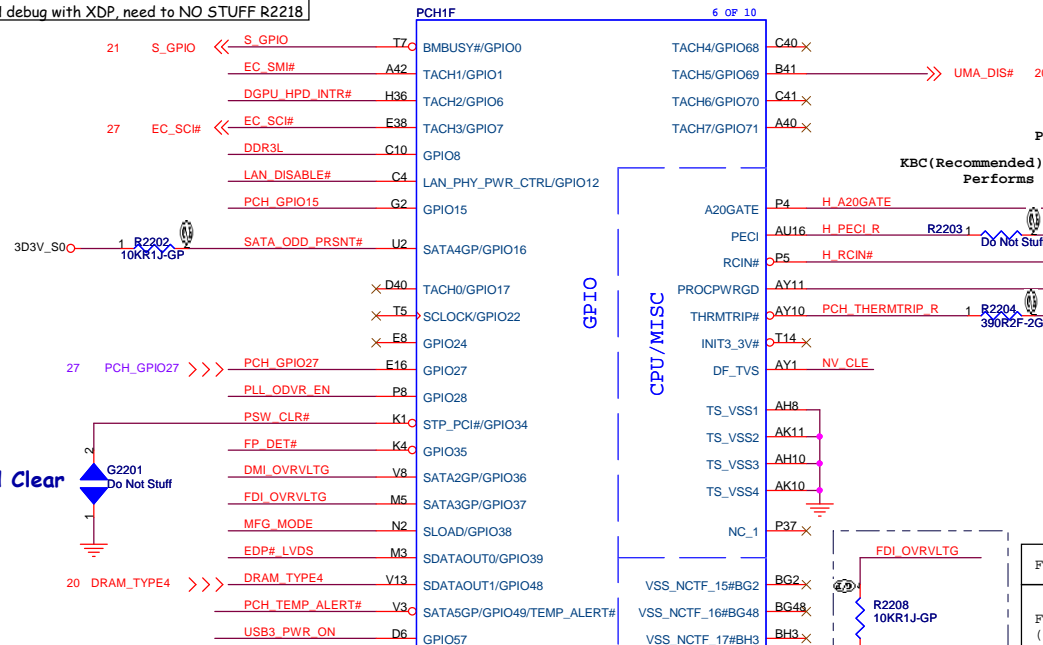
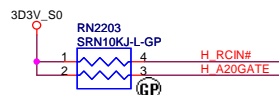
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Title **PCH (SPI/RTC/LPC/SATA/IHDA)**

Size A3	Document Number <b>M41 2SP</b>	Rev <b>SA</b>
Date: Tuesday, February 21, 2012	Sheet 21 of	100

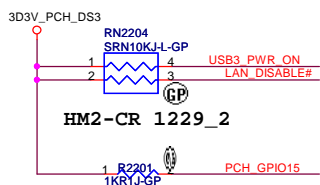
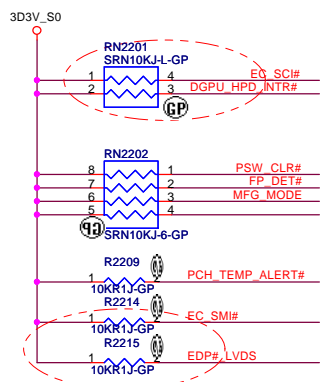
SSID = PCH

Note:  
For PCH debug with XDP, need to NO STUFF R2218



Pass Word Clear

HM2-CR SB 0117 by EDWIN  
request by layout



Do Not Stuff

NCTF TEST PIN:  
A4, A44, A45, A46, A5, A6, B3, B47,  
BD1, BD49, BE1, BE49, BF1, BF49,  
C2, C48, D1, D49, E1, E49, F1, F49

PANTHER-GP-NF 71.PANTH.00U

PCH:no Turbo control via PECI  
KBC(Recommended):EC collect all thermal data and  
Performs Turbo power control

FDI TERMINATION VOLTAGE OVERRIDE(Reserved)	
FDI_OVRVLTG (GPIO37)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE(Reserved)	
DMI_OVRVLTG (GPIO36)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Chip Enable(Reserved)	
ICC_EN# (GPIO8)	HIGH- DISABLED [DEFAULT] LOW - ENABLED

PLL ON DIE VR ENABLE	
PLL_ODVR_EN (GPIO28)	HIGH- DISABLED [DEFAULT] LOW - ENABLED

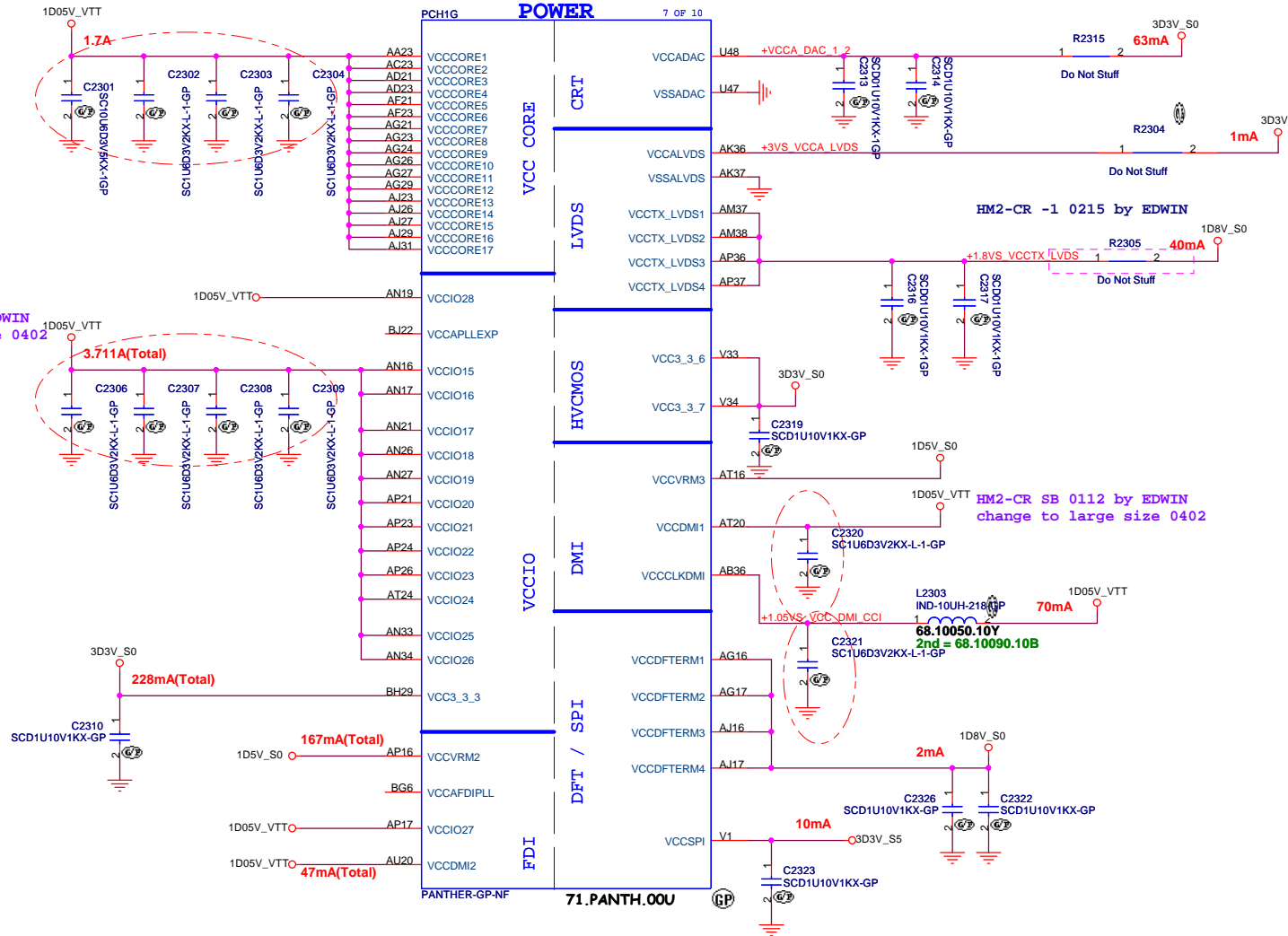
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Title PCH (GPIO/CPU)		
Size A3	Document Number M41 2SP	Rev SA
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PCFH1G	POWER		7 OF 10			
VCCCORE1	VCC CORE	CRT	VCCADAC			
VCCCORE2			VSSADAC			
VCCCORE3		LVDS	VCCALVDS			
VCCCORE4			VSSALVDS			
VCCCORE5			VCCTX_LVDS1			
VCCCORE6			VCCTX_LVDS2			
VCCCORE7			VCCTX_LVDS3			
VCCCORE8			VCCTX_LVDS4			
VCCCORE9			HVC MOS	VCC3_3_6		
VCCCORE10				VCC3_3_7		
VCCCORE11				DMI	VCCVRM3	
VCCCORE12					VCCDMI1	
VCCCORE13					VCCCLKDMI	
VCCCORE14					FDI	VCCDFTERM1
VCCCORE15						VCCDFTERM2
VCCCORE16						VCCDFTERM3
VCCCORE17			VCCDFTERM4			
VCCIO28	DFT / SPI	VCCSPI				
VCCAPLLEXP						
VCCIO15						
VCCIO16						
VCCIO17						
VCCIO18						
VCCIO19						
VCCIO20						
VCCIO21						
VCCIO22						
VCCIO23						
VCCIO24						
VCCIO25						
VCCIO26						
VCC3_3_3						
VCCVRM2						
VCCAFDIPLL						
VCCIO27						
VCCDMI2						



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Title			
<b>PCH (POWER1)</b>			
Size A3	Document Number		Rev
	<b>M41 2SP</b>		<b>SA</b>
Date:	Tuesday, February 21, 2012	Sheet 23 of	100

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SSID = PCH

HM2-CR SB 0112 by EDWIN  
change to large size lu 0402 10u 0603

HM2-CR SB 0112 by EDWIN  
change to large size lu 0402

HM2-CR SB 0112 by EDWIN  
change to large size lu 0402

HM2-CR SB 0112 by EDWIN  
change to large size lu 0603

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## POWER

## USB

## Clock and Miscellaneous

## PCI/GPIO/LPC

## SATA

## MISC

## CPU

## RTC

## HDA

HM2-CR SB 0112 by EDWIN  
change to large size lu 0402

Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rails

Va	Vb	Power-Up Requirement	Power-Down Requirement
VSREF_SUS	VCCSUS3_3	a) VCCSREF_SUS must be powered up before VCCSUS3_3 or after VCCSUS3_3 within 0.7 V. b) If VCCSREF_SUS is more than VCCSUS3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) VSREF_SUS must be powered down after VCCSUS3_3 or before VCCSUS3_3 within 0.7 V.
VSREF	VCC3_3	a) VSREF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V. b) For power up, if VCCSREF is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) VSREF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)

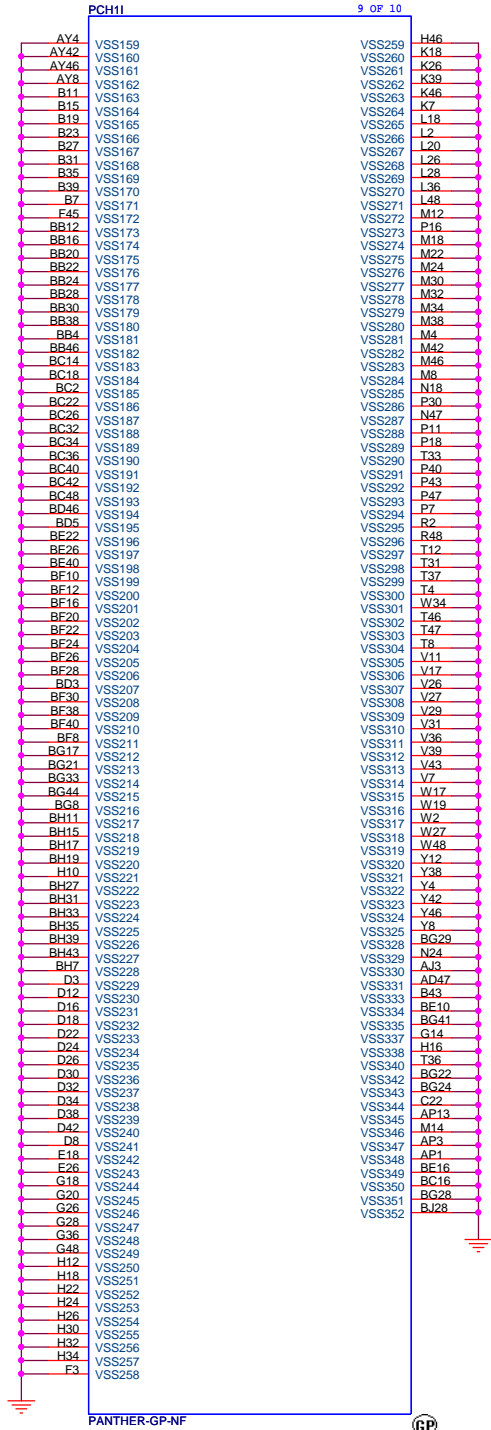
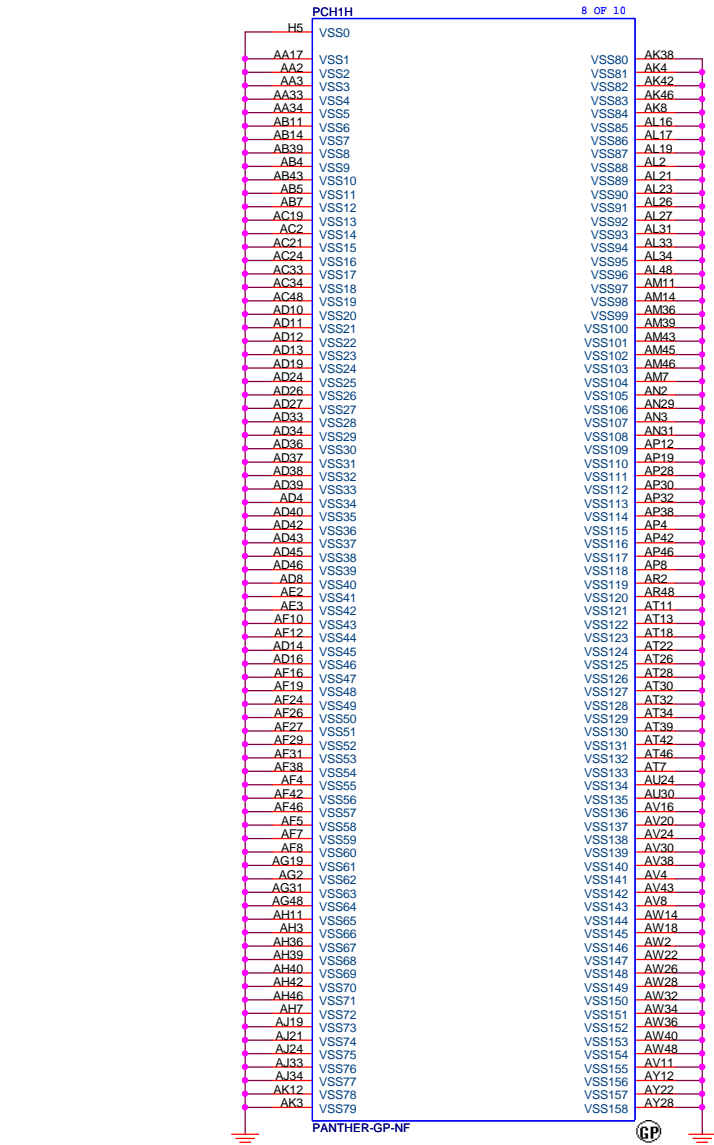
Elpida 1333 4G DS3 NonSSD 65W

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Title	PCH (POWER2)		
Size	Document Number		Rev
A3	M41 2SP		SA
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SSID = PCH



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Title PCH (VSS)

Size A3 Document Number M41 2SP Rev SA

Date: Tuesday, February 21, 2012 Sheet 25 of 100

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Title <div>Clock(colay)</div>		
Size <div>A4</div>	Document Number <div>SM30 HS</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>26</div> of <div>102</div>



### *Thermal sensor P2800*



optional

$R_{up}$

Option 1: OTZ=95°C → ADJ=3.3V

Option 2: OTZ=85°C → ADJ=Floating

Option 3: OTZ=90°C → ADJ=GND

optional

$R_{down}$

2N3904

2200pF

3.0V to 3.6V

0.1μF

100kΩ

Thermal Shutdown

Thermal Reporting

Thermal Reporting

VCC

ADJ

OTZ

P2800EB0

DXP

DXN

TDL

TDR

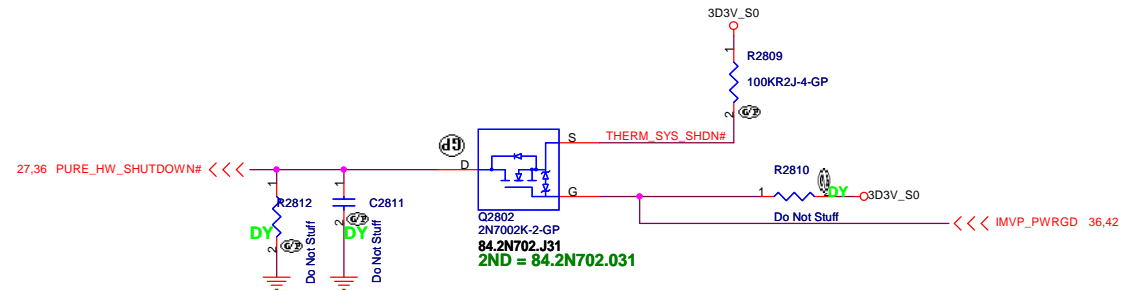
GND

VCC

KBC

GND

Note that  $R_{up}$  and  $R_{down}$  are optional for the purpose of circuit backward compatible with P2800EA1 designs. For new designs the two resistors can be replaced by short circuit wherever applicable





AUDIO OP AMPLIFIER

Blanking

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Title <div>Audio AMP</div>		
Size <div>A4</div>	Document Number <div>SM30 HS</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>30</div> of <div>102</div>

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緯創資通

Wistron Corporation

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Title

AR8158

Size  
A3

Document Number  
SM30 HS

Rev  
-SA

Date: Tuesday, February 21, 2012

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Card reader move to small board

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Title <div>RTS5159 (CARD READER)</div>		
Size <div>A4</div>	Document Number <div>SM30 HS</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>32</div> of <div>102</div>



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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>SM30 HS</div>	Rev <div>-SA</div>
Date: Tuesday, February 21, 2012		Sheet 33 of 102

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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>SM30 HS</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>34</div> of <div>102</div>

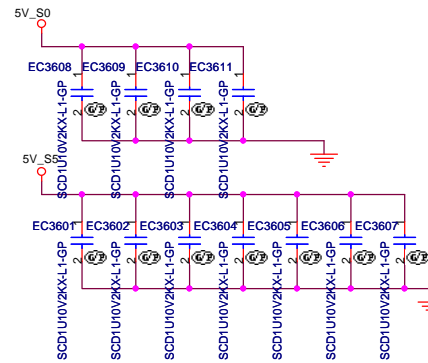
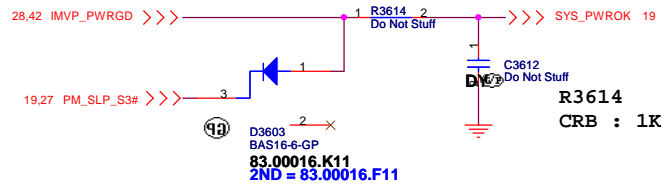
# Blanking

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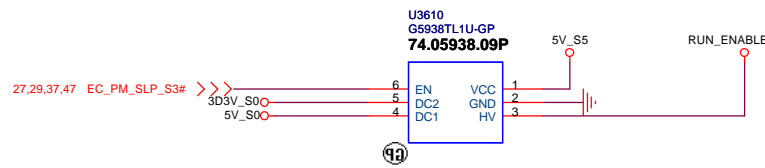
Elpida 1333 4G DS3 NonSSD 65W

Title		Wistron Corporation	
Size		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Date:		Rev	
Tuesday, February 21, 2012		-SA	
Sheet		102	
35		of	
1			

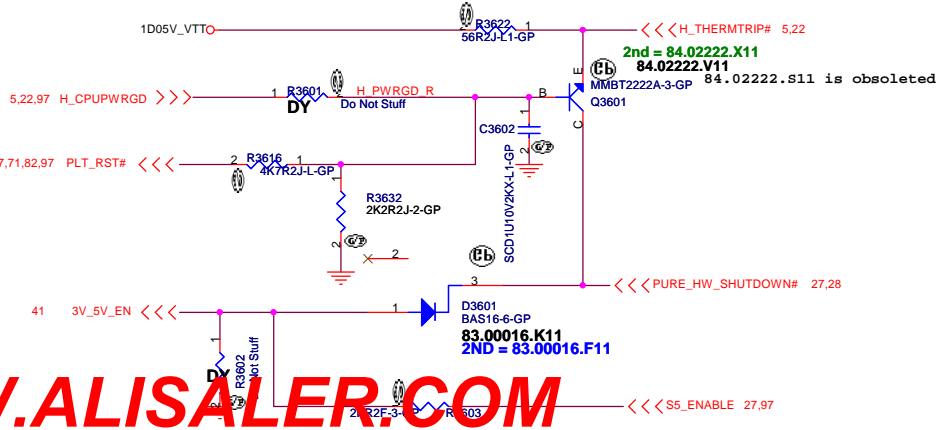
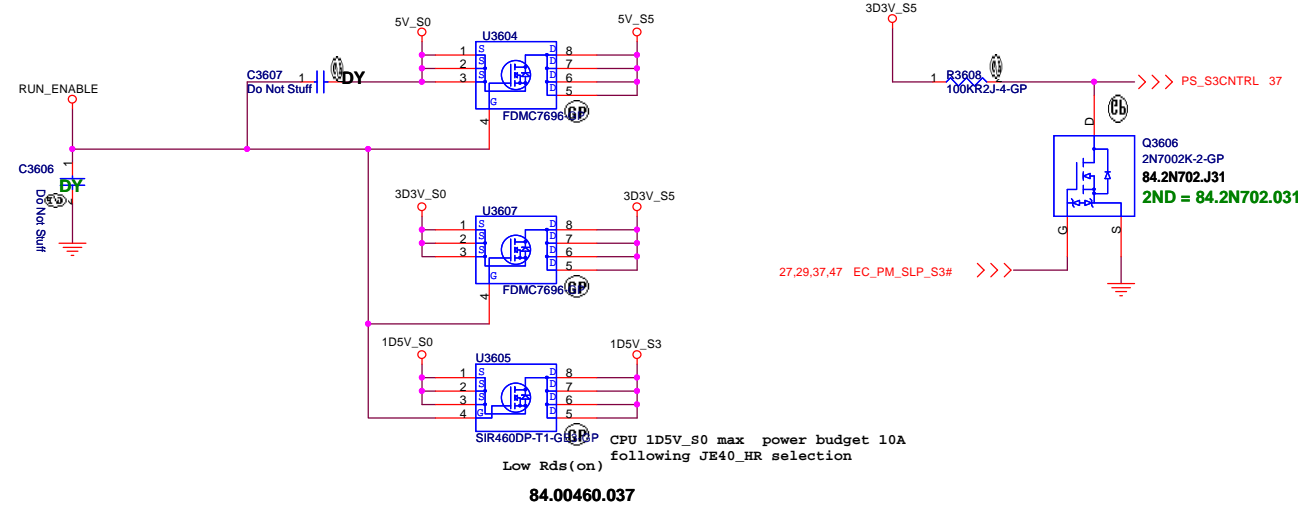
# Power Sequence



## ANNIE Run Power



Modify the MOS package for placement



DDR\_VREF\_S3

R3707 100k Do Not Solder

DY Q3708 A03418-GP

K1 84.03418.031

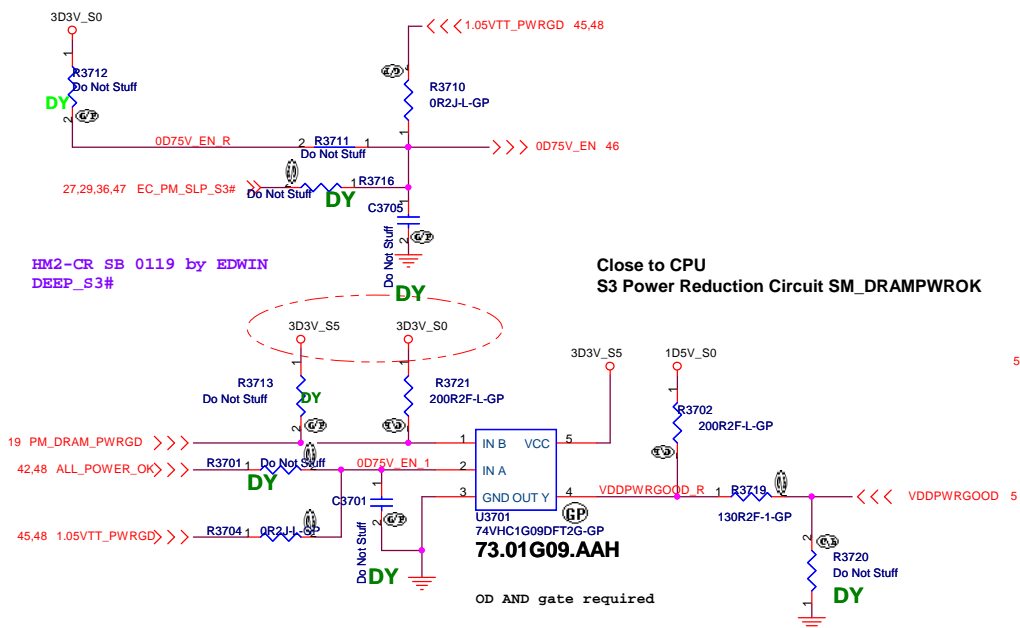
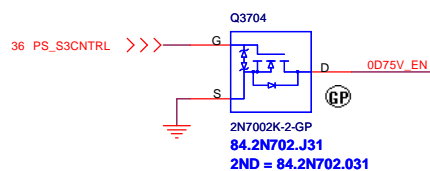
R3705 100kR2J-4GP

package => SOT-23

A03468->Rds(on) <155-ohm  
2N702 Rds(on)->3-ohm

>>> +V\_SM\_VREF\_CNT 9

<<< EC\_PM\_SLP\_S3# 27.29,36,47



For U3701 not OD AND gate  
R3719 to 64.15015.6DL  
R3720 to 64.75005.6DL  
R3702 to DY

SMD MROK must have a maximum of 15ns rise or fall time over  $V_{DD} \pm 0.55 \pm 200\text{mV}$  and the edge must be monotonic

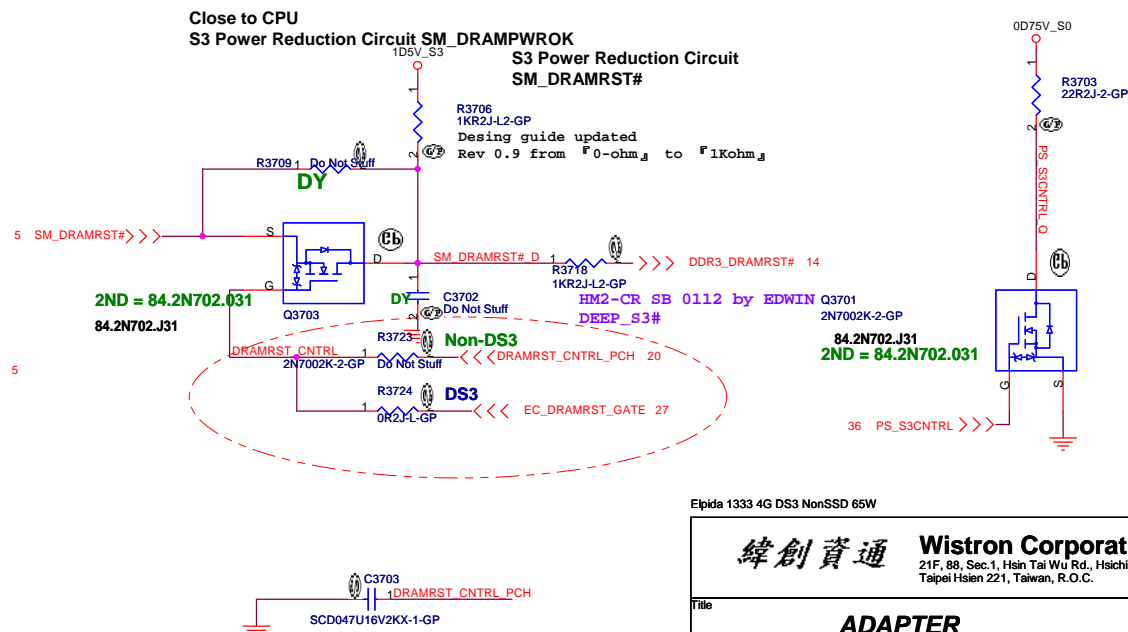
Close to CPU  
S3 Power Reduction Circuit SM\_DRAMPWROK

105V\_S3

S3 Power Reduction Circuit  
SM\_DRAMRST#

R3706  
1K2JH2-GP

Desing guide updated  
Rev 0.9 from F0-ohm<sub>s</sub> to F1Kohm<sub>s</sub>



Elpida 1333 4G DS3 NonSSD 65W

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Title

## ADAPTER

Size

Document Number

SM30\_HS

Date: Tuesday, February 21, 2012

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Move to small board

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Title <div>DCIN JACK</div>		
Size <div>A4</div>	Document Number <div>SM30 HS</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>38</div> of <div>102</div>

Move to small board

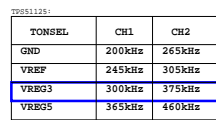
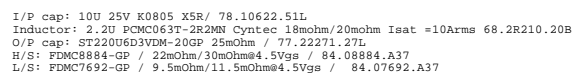
Elpida 1333 4G DS3 NonSSD 65W

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
BATT CONN		
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A4	SM30 HS	-SA
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Move to small board



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TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

I/P cap:10U 25V K0805 X5R/ 78.10622.51L  
Inductor: 1.50UH PCMC104T-1R5 Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J  
O/P cap: ST220U6D3VDM-20GP 25mOhm / 77.22271.27L  
H/S: S1R172DP-T1-GE3-GP / 10.30mOhm/12.40mOhm@4.5Vgs / 84.00172.037  
L/S: S1R460DP-T1-GE3-GP / 4.90mOhm/6.10mOhm@4.5Vgs / 84.00460.037

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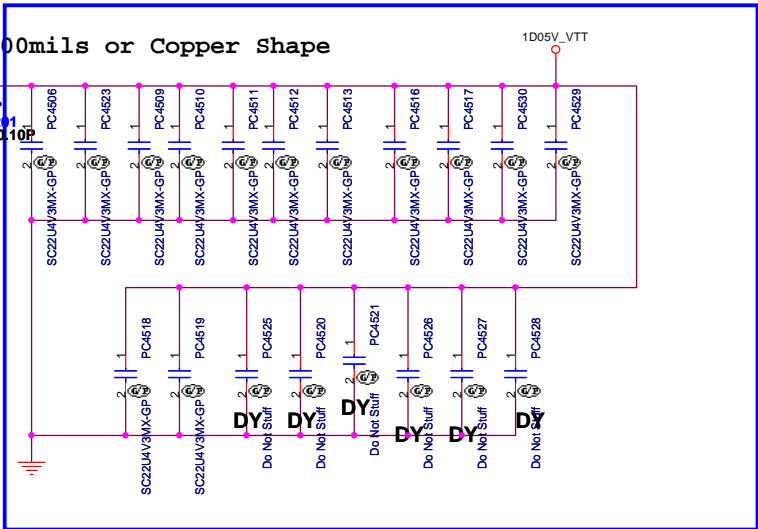




```

Delete the old version VT386F cir

```



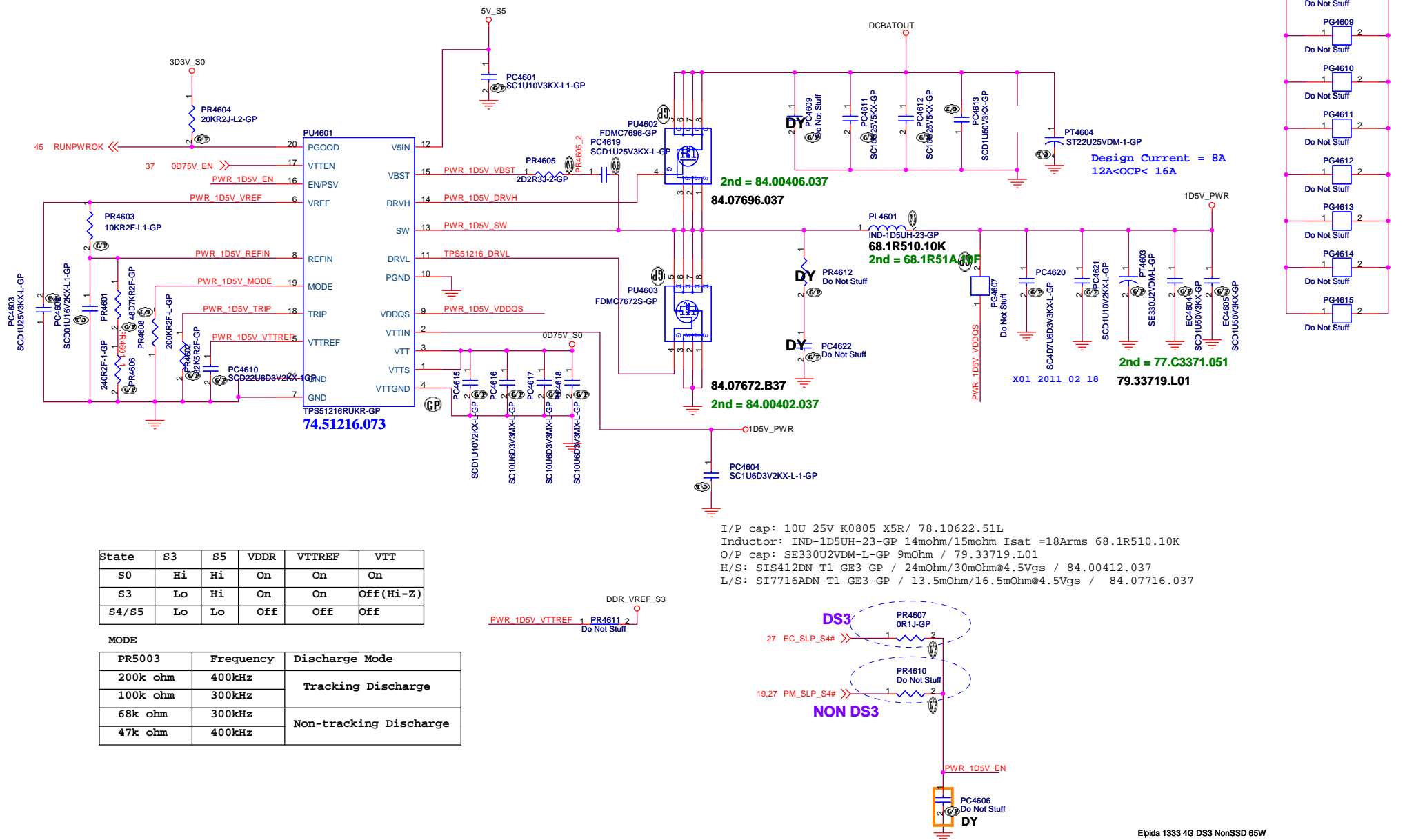
PL4502  
1 2  
COIL-D20UH-GP  
68.R2010.2  
2nd = 68.R2010

Change to 0603\_4v

The diagram shows the LCC package with two pins highlighted: PR4510 and PR4517. Pin PR4510 is connected to VCCIO\_SENSE, and pin PR4517 is connected to VSSIO\_SENSE. The text "Do Not Stuff PR4510" and "Do Not Stuff PR4517" is present next to the pins. A note at the bottom states: "Change 0R PAD to 0R and DY".

Change OR PAD to OR and DY

SSID = PWR.Plane.Regulator 1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE		
PR5003	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: IND-1D5UH-23-GP 14mohm/15mohm Isat =18Arms 68.1R510.10K  
O/P cap: SE330U2VDM-L-GP 9mOhm / 79.33719.L01  
H/S: SIS412DN-T1-GE3-GP / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
L/S: SI7716ADN-T1-GE3-GP / 13.5mOhm/16.5mOhm@4.5Vgs / 84.07716.037

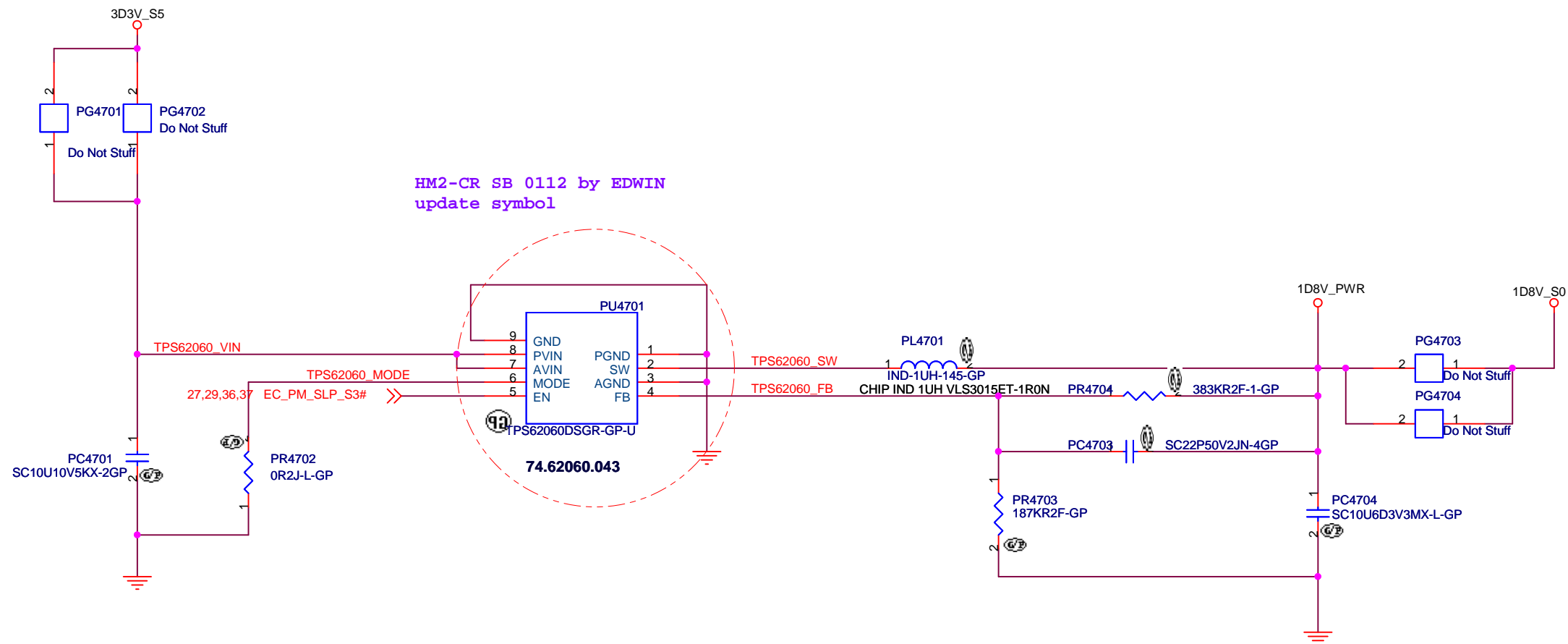
Elpida 1333 4G DS3 NonSSD 65W

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Title			
<b>TPS51116 +1.5V SUS</b>			
Size A3	Document Number		Rev
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SSID = PWR.Plane.Regulator\_1p8v



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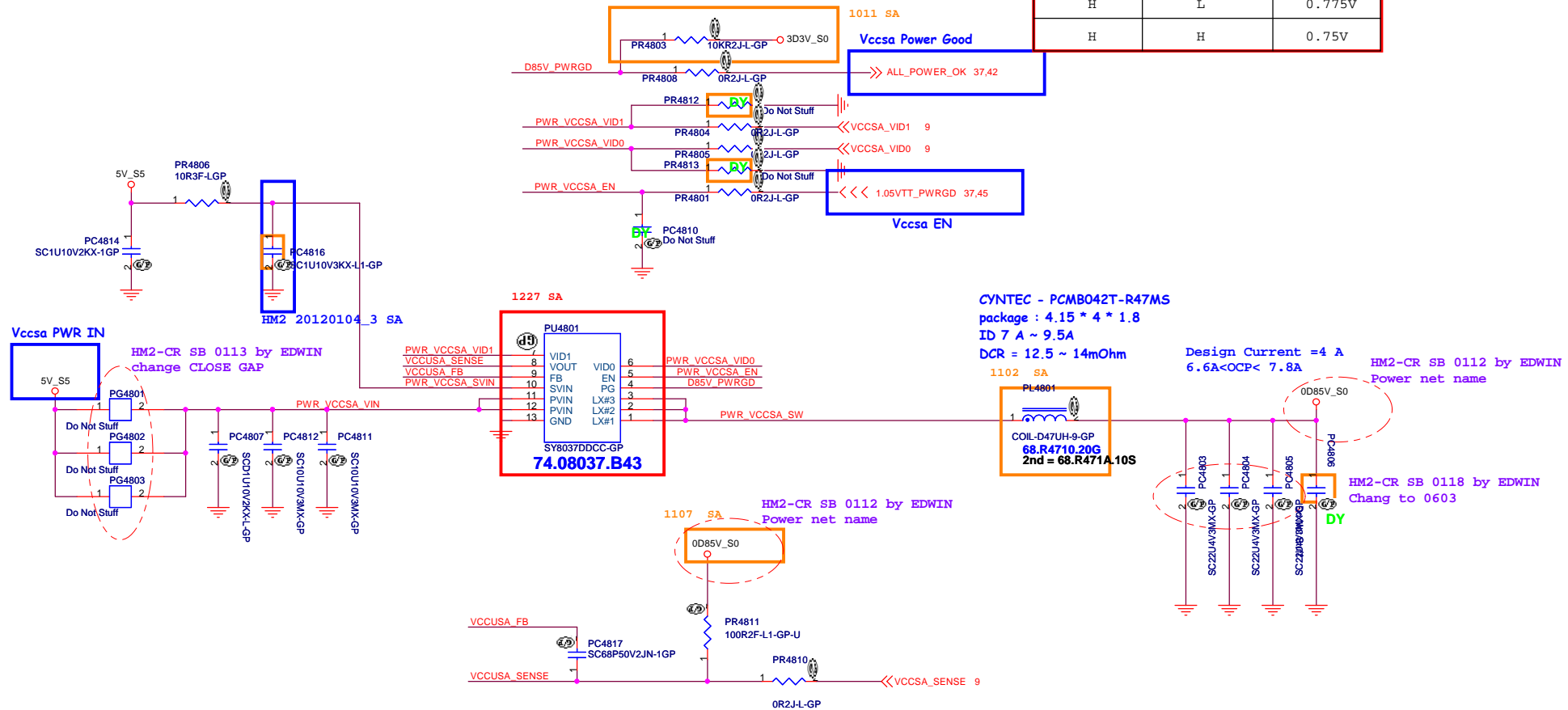
Title DC CONVERTER\_1D8V

Size A4	Document Number SM30 HS	Rev SA
------------	----------------------------	-----------

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# SY8037 for VCCSA

VID0	VID1	VCCSA ULV
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V



Epida 1333 4G DS3 NonSSD 65W

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Title **TPS51461\_VCCSA**

Size A3 Document Number

**SM30 HS**

Rev

**SA**

Date: Tuesday, February 21, 2012

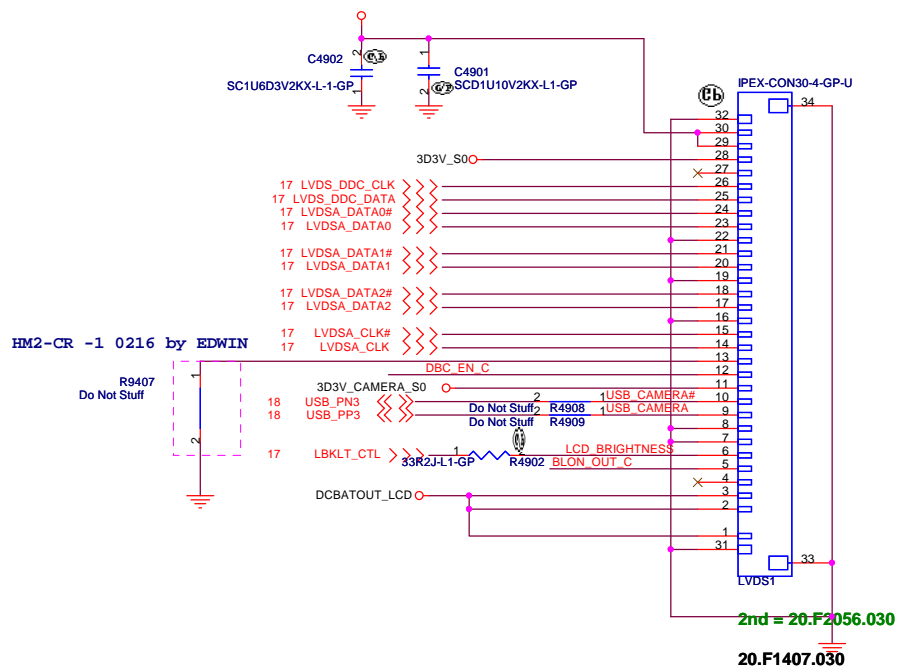
Sheet 48 of 102



**SSID = VIDEO**

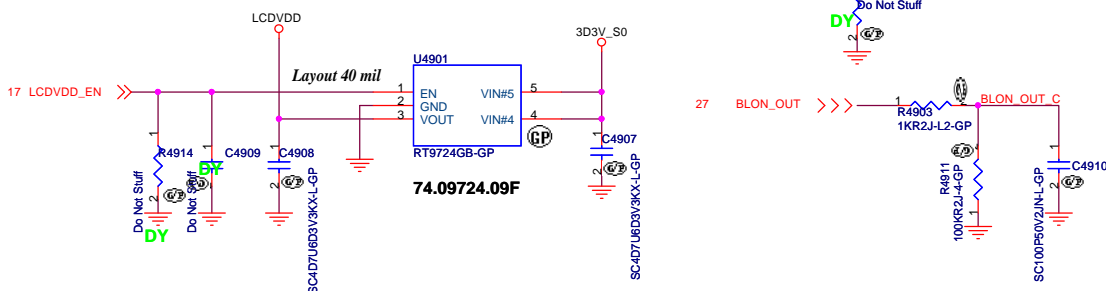
Reverse the pin define becасue of cable issue

**LVDS CONNECTOR**  
LCDVDD

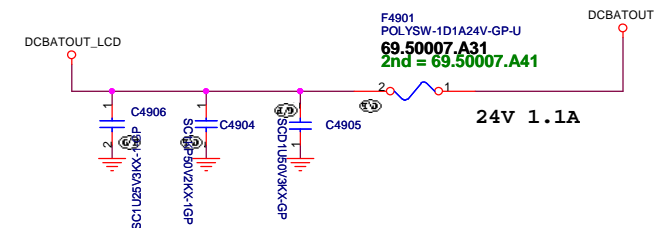


**SSID = VIDEO**

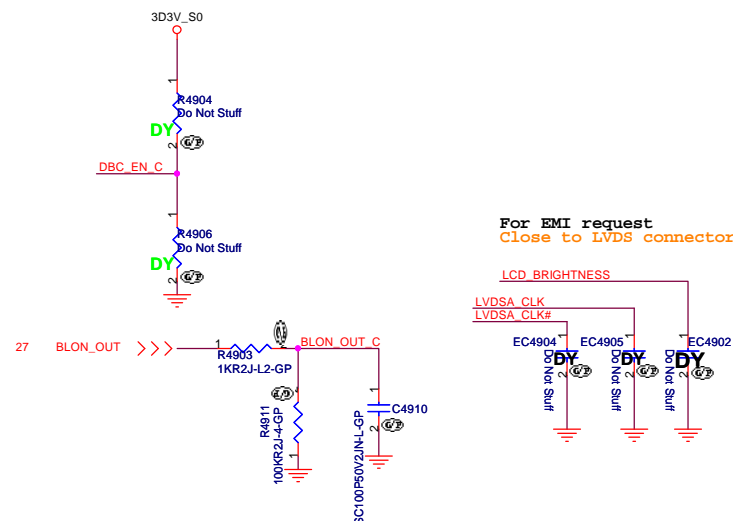
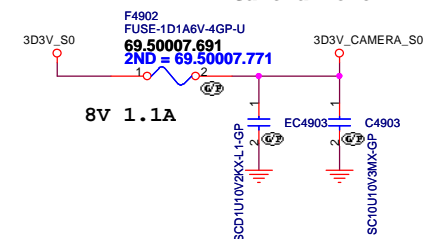
LCD POWER for ANNIE



## INVERTER POWER



## Camera Power



For EMI request  
Close to LVDS connector

The diagram shows three digital signals over time for three EC4905 chips. The signals are:

- LCD\_BRIGHTNESS**: A purple line that starts high, then drops to low and remains low.
- LVDS\_A\_CLK**: A red line that starts high, then drops to low and remains low.
- LVDS\_A\_CLK#**: A red line that starts high, then drops to low and remains low.

Each chip has a 'Do Not Sniff' label with a crossed-out sniff icon. The chips are labeled EC4904, EC4905, and EC4902 from left to right.

Elpida 1333 4G DS3 NonSSD 65W

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Title			
<b>LCD Connector</b>			
Size A3	Document Number		Rev
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Date	Tuesday, February 21, 2012		Sheet 49 of 102

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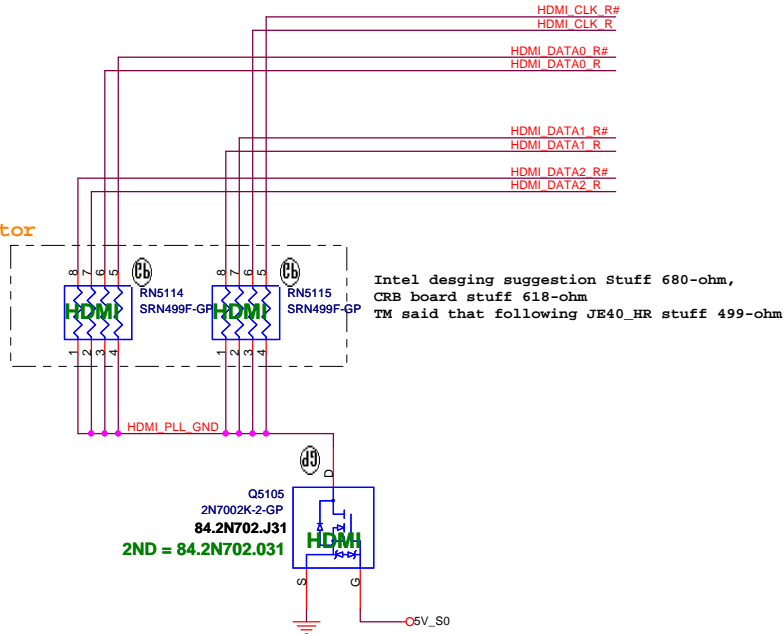
Pull High 5V Design on CRT Board  
CRT DDCDATA & DDCCLK level shift

SSID = VIDEO

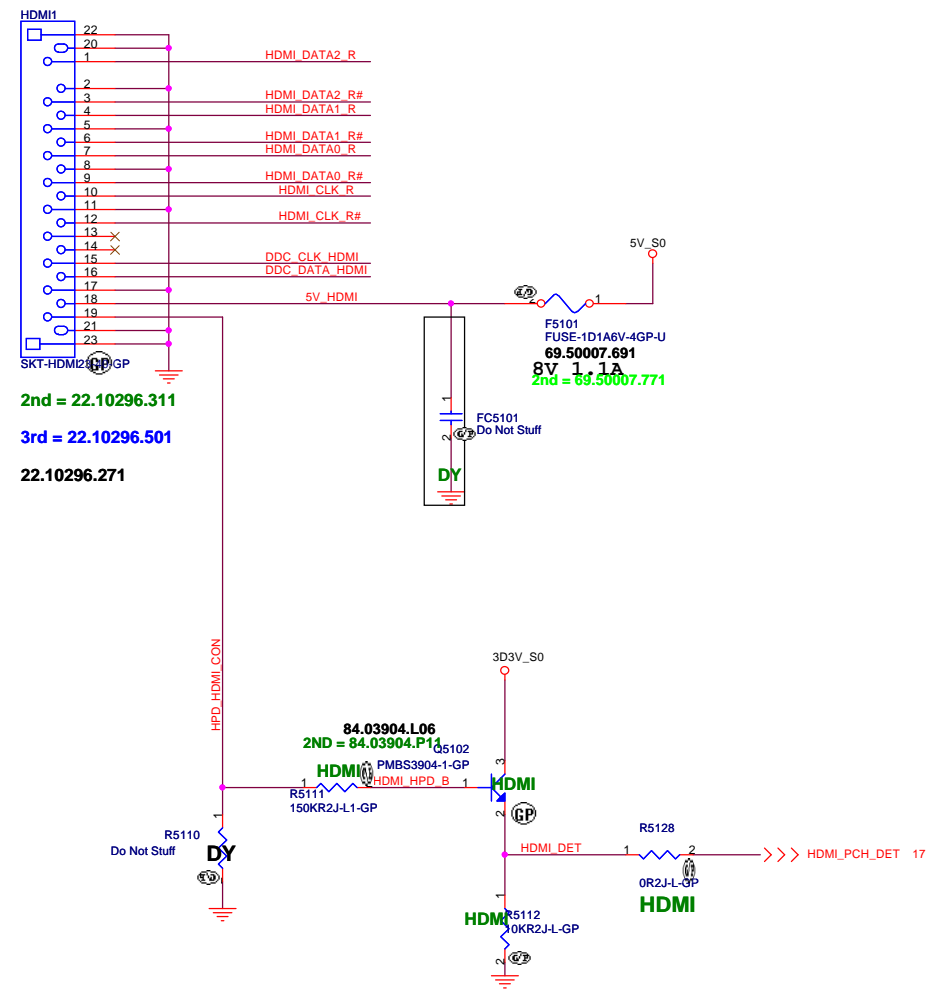
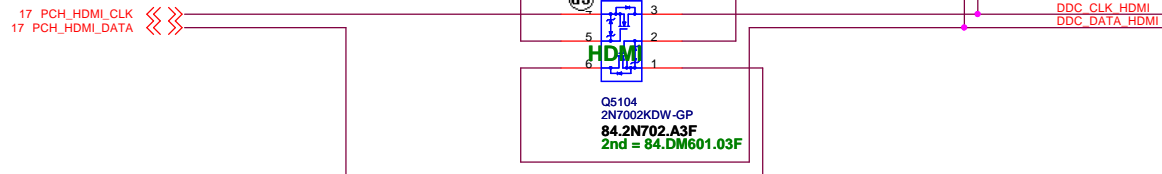
# HDMI Level Shifter & CONNECTOR

17 HDMI\_CLK\_R# >>>  
17 HDMI\_CLK\_R >>>  
17 HDMI\_DATA0\_R# >>>  
17 HDMI\_DATA0\_R >>>  
17 HDMI\_DATA1\_R# >>>  
17 HDMI\_DATA1\_R >>>  
17 HDMI\_DATA2\_R# >>>  
17 HDMI\_DATA2\_R >>>

Close to HDMI Connector



Close to Level Shift



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Title		HDMI Level Shifter/Connector	
Size	Document Number	Rev	-SA
A3	SM30_HS		
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Title

eDP

Size  
A3

Document Number  
SM30\_HS

Rev  
-SA

Date: Tuesday, February 21, 2012

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Elpida 1333 4G DS3 NonSSD 65W

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>S-VIDEO</div>		
Size <div>A4</div>	Document Number <div>SM30 HS</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>53</div> of <div>102</div>

(Blanking)

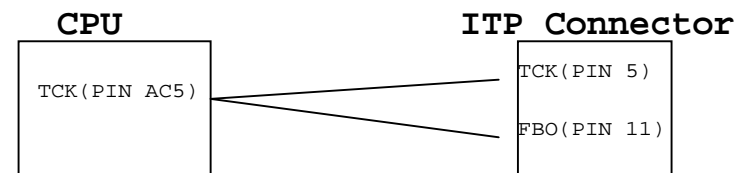
Elpida 1333 4G DS3 NonSSD 65W

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>SM30 HS</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>54</div> of <div>102</div>

SSID = User.Interface

# ITP Connector

H\_CPURST# use pull-up Resistor close  
ITP connector 500 mil ( max ),  
others place near CPU side.



Elpida 1333 4G DS3 NonSSD 65W

緯創資通

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Title

**ITP**

Size  
A4

Document Number

**SM30 HS**

Rev

**-SA**

Date: Tuesday, February 21, 2012

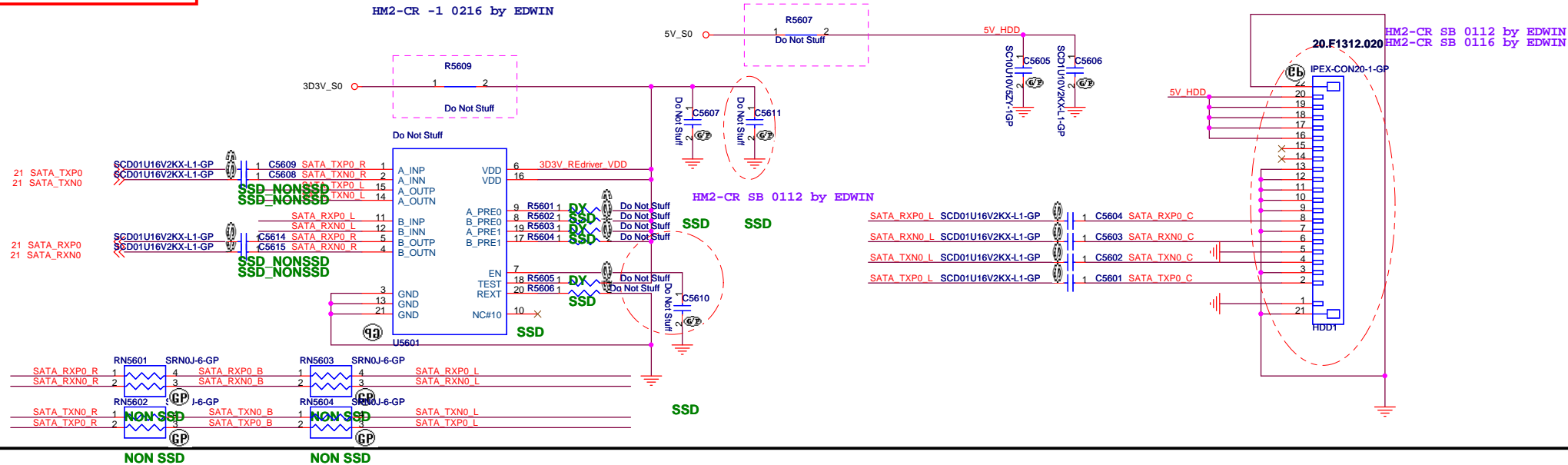
Sheet 55 of 102

SSID = SATA

# SATA HDD Connector

HM2-CR -1 0216 by EDWIN

HM2-CR -1 0216 by EDWIN



## ODD Connector

Without ODD

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File		HDD/ODD	
Size	Document Number	Rev	
A3	SM30 HS	-SA	
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ESATA Power

USB CHARGER

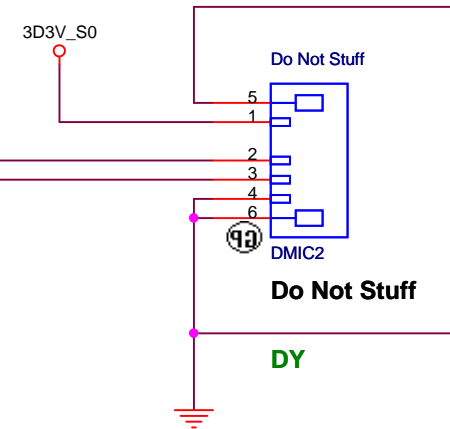
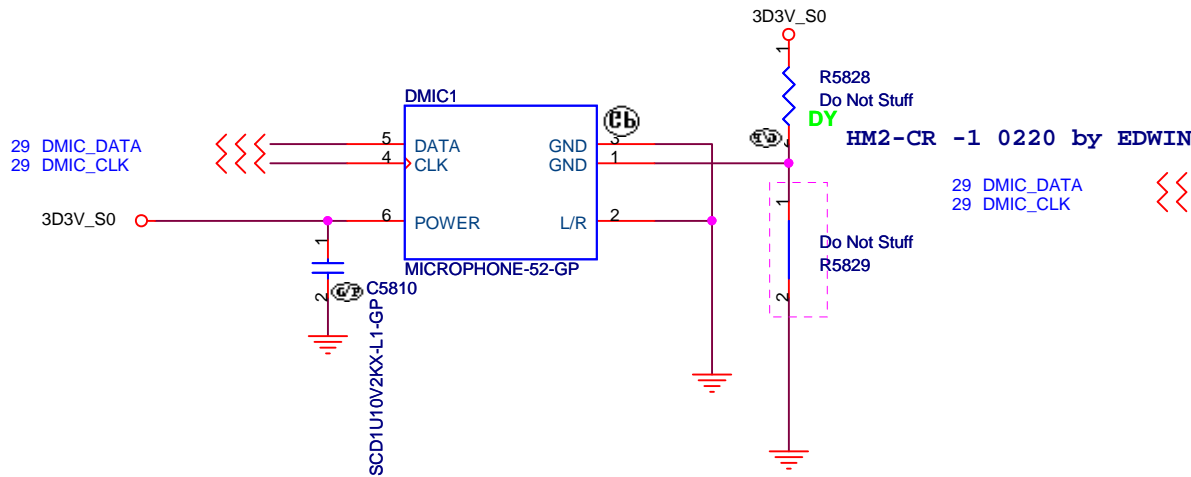
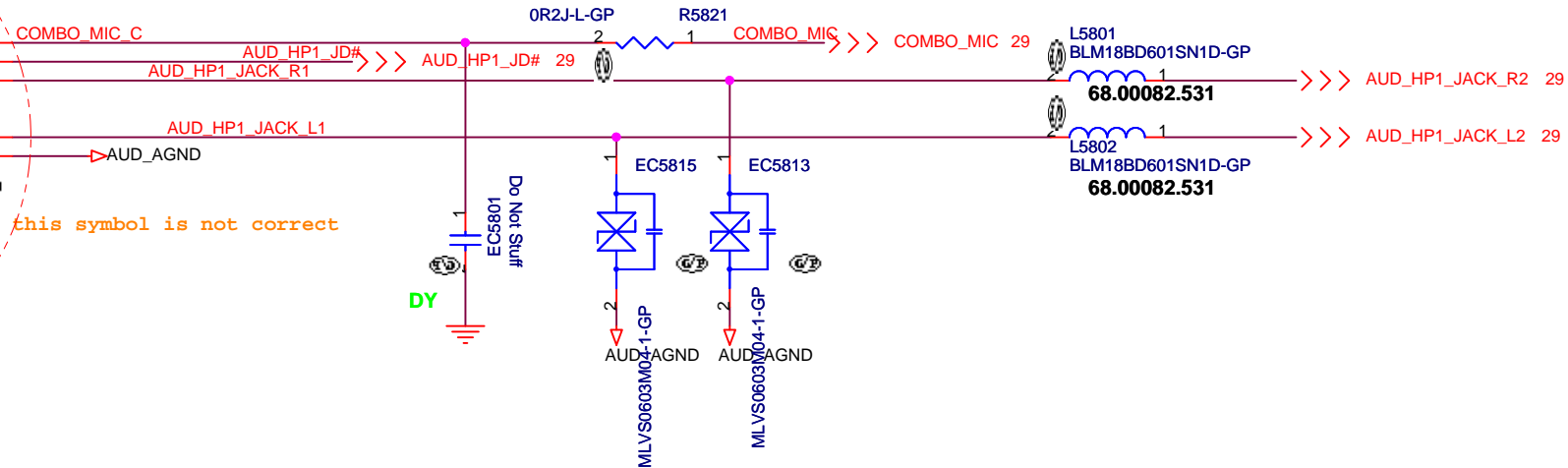
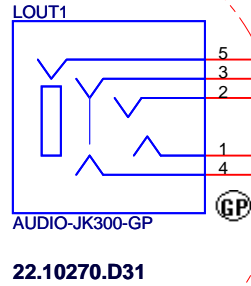
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Elpida 1333 4G DS3 NonSSD 65W

<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
E-SATA/USB CHARGER		
Size	Document Number	Rev
A3	SM30_HS	-SA
Date:	Tuesday, February 21, 2012	Sheet 57 of 102

SSID = AUDIO

HM2-CR SB 0112 by EDWIN  
update symbol



Elpida 1333 4G DS3 NonSSD 65W

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio Jack

Size  
A4

Document Number

SM30 HS

Rev

-SA

Date: Tuesday, February 21, 2012

Sheet 58 of 102

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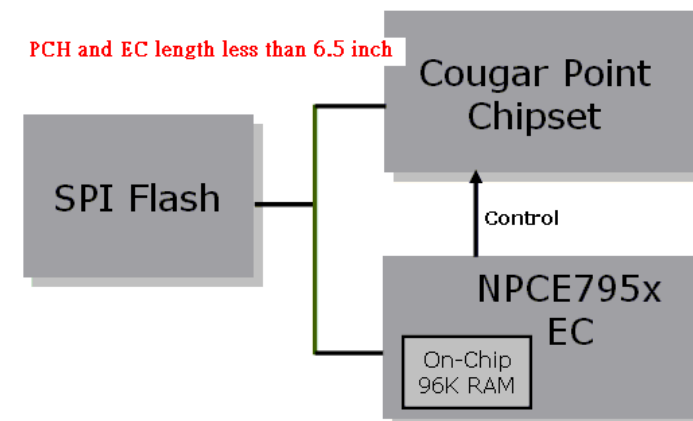
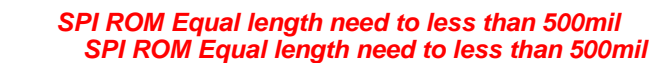
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

# Without LAN

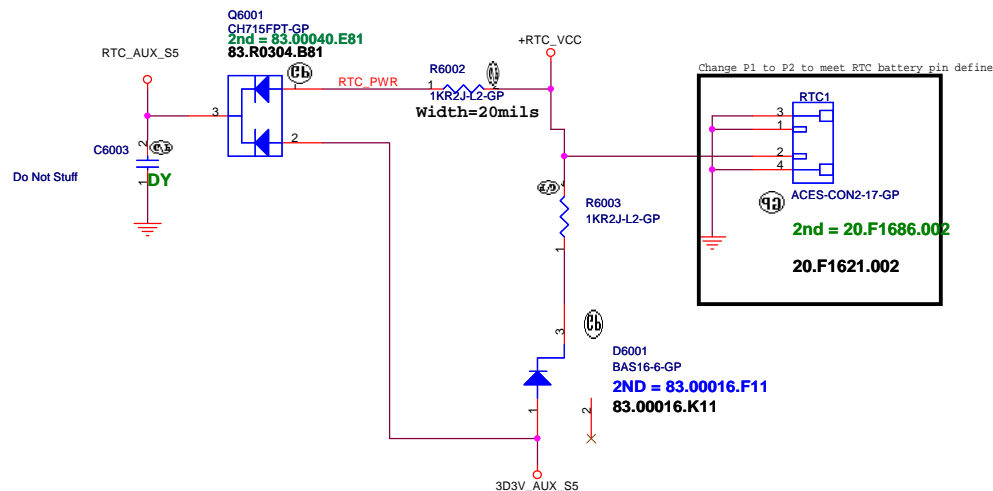
Elpida 1333 4G DS3 NonSSD 65W

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>LAN CONNECTOR</div>		
Size <div>A4</div>	Document Number <div>SM30 HS</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>59</div> of <div>102</div>

```
SSID = Flash.ROM
```



## SSID = RBATT

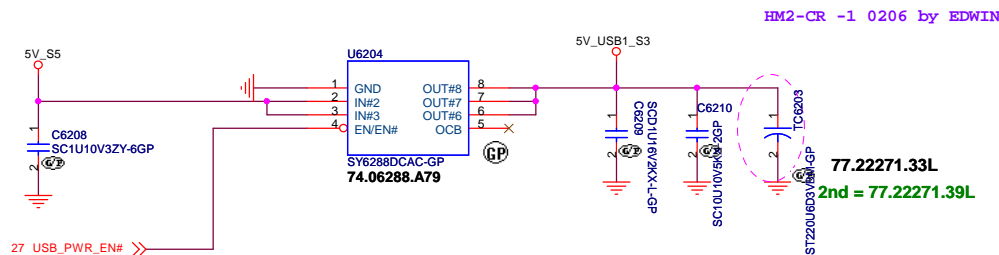


## RTC battery charger circuit

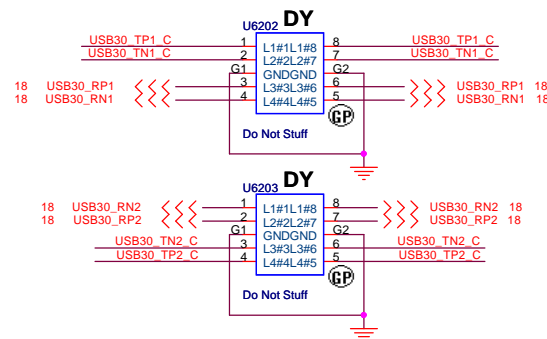
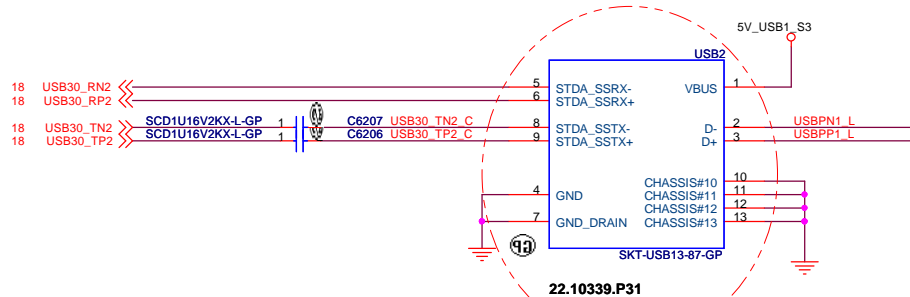
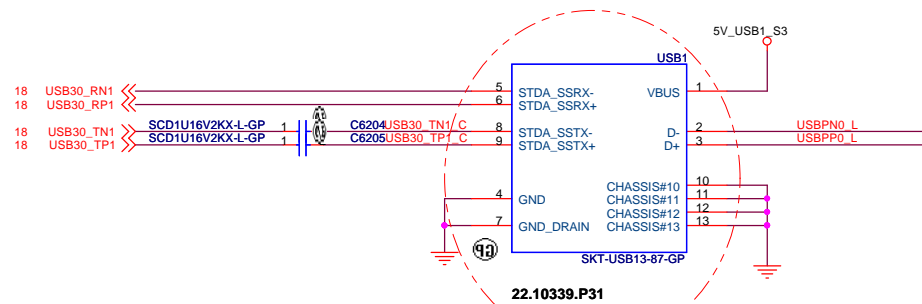
SSID = USB

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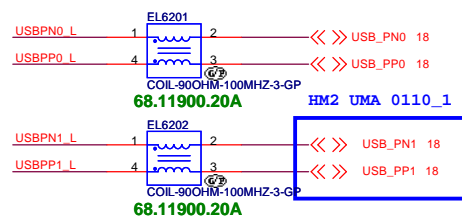
Elpida 1333 4G DS3 NonSSD 65W		
<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
USB Power SW		
Size	Document Number	Rev
A3	SM30_HS	-SA
Date:	Tuesday, February 21, 2012	Sheet 61 of 102



HM2-CR -1 0218 by EDWIN



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



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Title		USB 3.0 Port	
Size	Document Number	Rev	
A3		Rogue	SA
Date:	Tuesday, February 21, 2012	Sheet	62 of 100

SSID = User.Interface  
Bluetooth Module conn.

Without BT

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Title

**Bluetooth**

Size  
A4

Document Number

**SM30 HS**

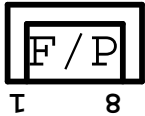
Rev  
-SA

Date: Tuesday, February 21, 2012

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Finger printer

JE40 delete FP function



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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
RESERVED		
Size	Document Number	Rev
A4	SM30 HS	-SA
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SSID = Wireless

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Title		
MINICARD(WLAN)/ITP CONN		
Size	Document Number	Rev
A4	SM30 HS	-SA
Date: Tuesday, February 21, 2012		Sheet 65 of 102

SSID = Wireless

Blanking

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Title

**WWAN Connector**

Size  
A4

Document Number

**SM30 HS**

Rev

**-SA**

Date: Tuesday, February 21, 2012

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# Blanking

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Title		
M-SATA		
Size	Document Number	Rev
A4	SM30 HS	-SA
Date:	Tuesday, February 21, 2012	Sheet 67 of 102

SSID = User.Interface

*Move to power board*

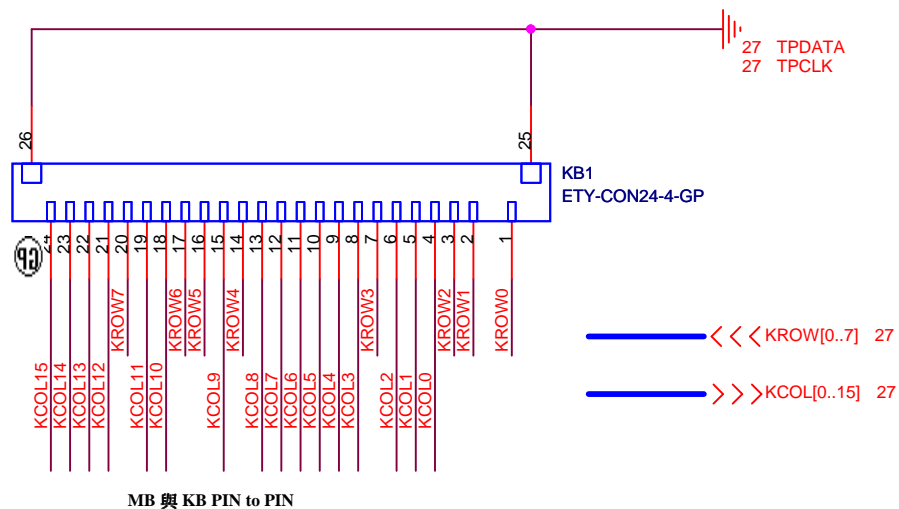
for factory test

Elpida 1333 4G DS3 NonSSD 65W

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
LED Bard/Power Button		
Size	Document Number	Rev
Custom	SM30 HS	-SA
Date:	Tuesday, February 21, 2012	Sheet 68 of 102

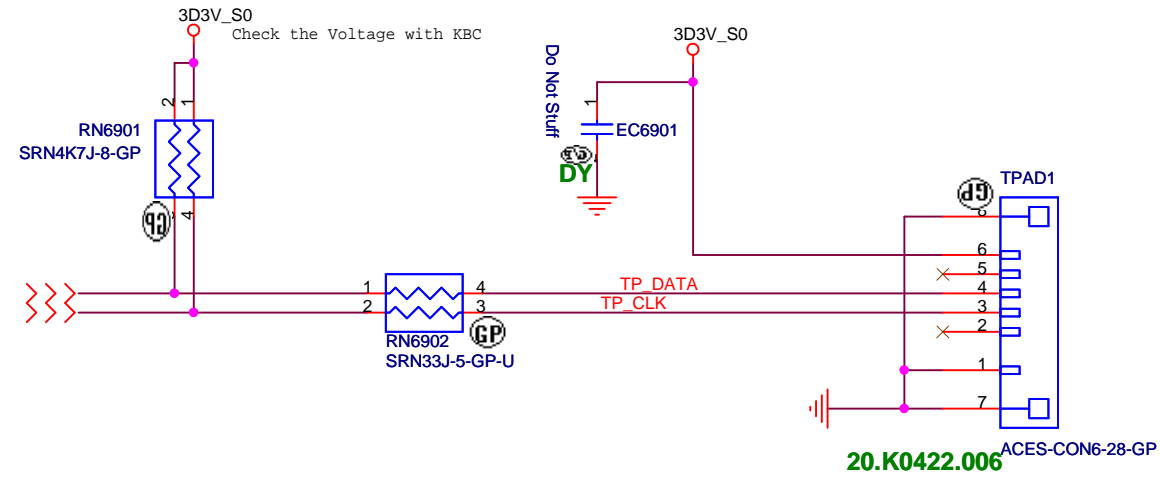
SSID = KBC

# Internal KeyBoard Connector



Change KB from 下接觸 to 上接觸  
KB Pin define need to check again

# TOUCH PAD



Change back to 1mm pin pitch connector  
Switch the pin order SA

D

D

C

C

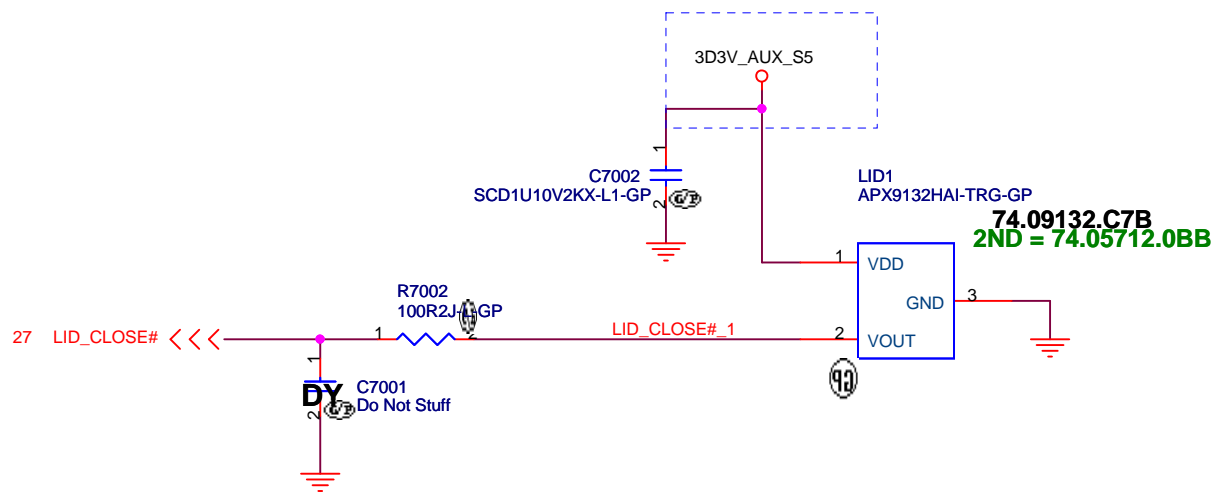
B

B

A

A

Change from 3D3V\_AUX\_KBC to 3D3V\_AUX\_S5



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Title

**Hall Sensor**

Size  
A4

Document Number

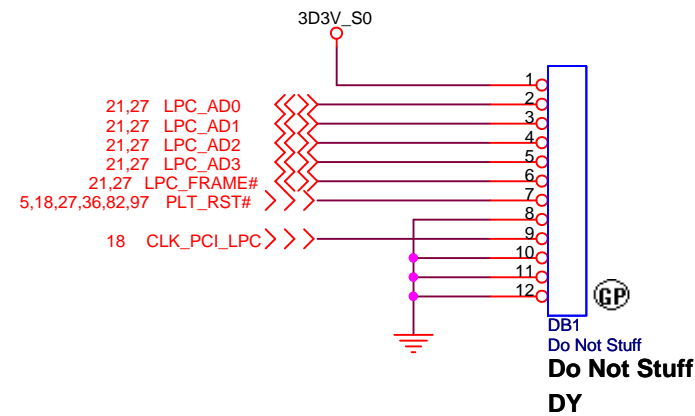
**HMA40 HR**

Rev

**-SA**

Date: Tuesday, February 21, 2012

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Title

***Dubug connector***

Size  
A4

Document Number

**HMA40 HR**

Rev

**-SA**

Date: Tuesday, February 21, 2012

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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>HMA40 HR</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>72</div> of <div>102</div>



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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>SM30 HS</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>73</div> of <div>102</div>

# SD/XD/MS Card Reader

Card reader move to small board

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Title <div>CARD Reader CONN</div>		
Size <div>A4</div>	Document Number <div>SM30 HS</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>74</div> of <div>102</div>

SSID = ExpressCard

+1.5V\_CARD Max. 650mA, Average 500mA.  
+3.3V\_CARD Max. 1300mA, Average 1000mA  
+3.3V\_CARDAUX Max. 275mA

( Blanking )

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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>HMA40 HR</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>76</div> of <div>102</div>

(Blanking)

Elpida 1333 4G DS3 NonSSD 65W

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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>HMA40 HR</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>77</div> of <div>102</div>

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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>HMA40 HR</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>78</div> of <div>102</div>

SSID = User.Interface

## Free Fall Sensor

### Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Delete G Sensor Function

### Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

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Elpida 1333 4G DS3 NonSSD 65W

**緯創資通**

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Title

**Free Fall Sensor**

Size  
A4

Document Number

**HMA40 HR**

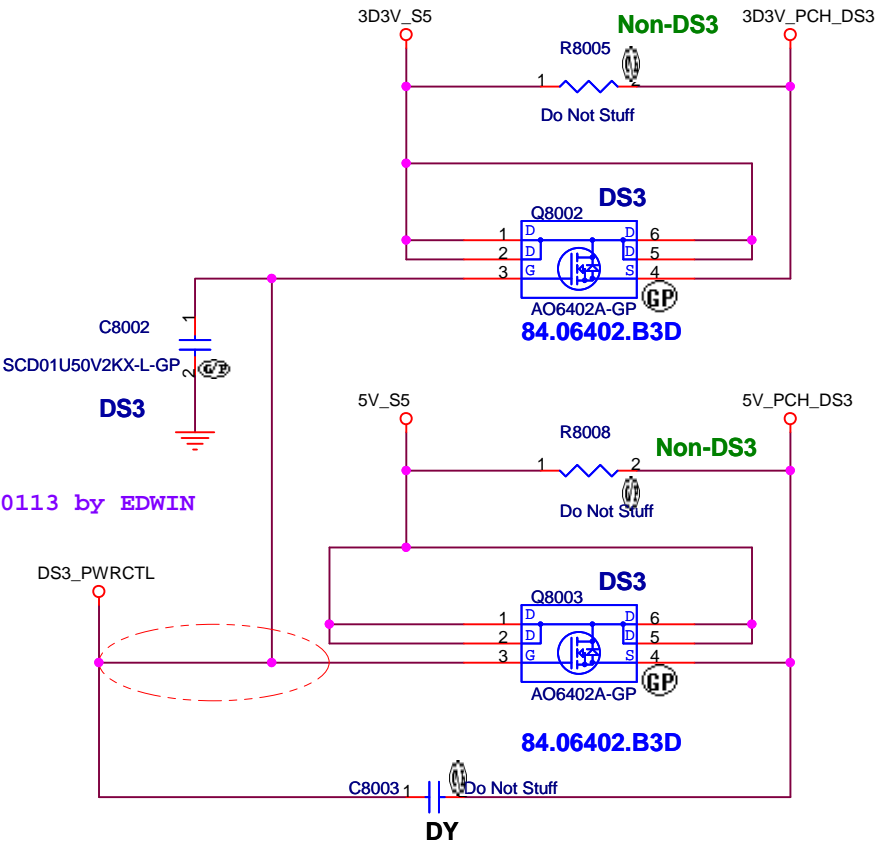
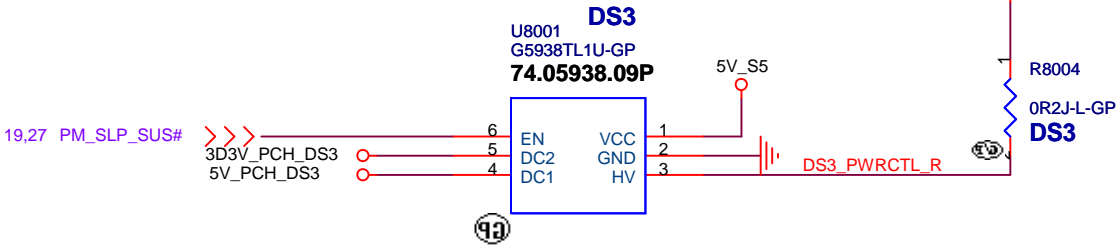
Rev

**-SA**

Date: Tuesday, February 21, 2012

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SA\_20111013\_DS3



Elpida 1333 4G DS3 NonSSD 65W

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Title			<b>Reserved</b>	
Size A4	Document Number <b>HMA40 HR</b>		Rev <b>-SA</b>	
Date: Tuesday, February 21, 2012		Sheet 80	of 102	

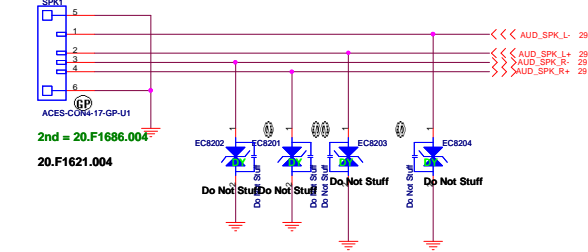


(Blanking)

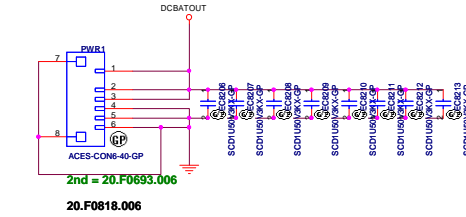
Elpida 1333 4G DS3 NonSSD 65W

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>HMA40 HR</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>81</div> of <div>102</div>

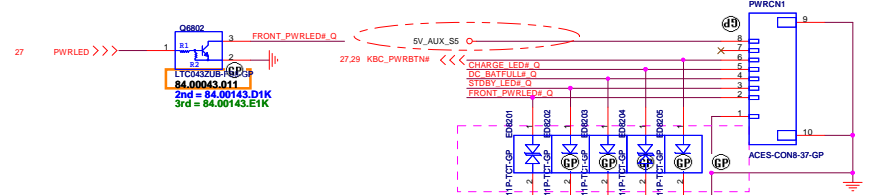
## Change to 4 pin connector



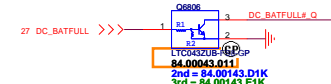
## Change the connection



## HM2-CR SB 0113 by EDWIN

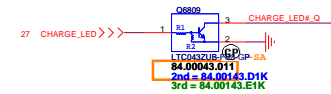


## Battery LED2(DC\_BATFULL)

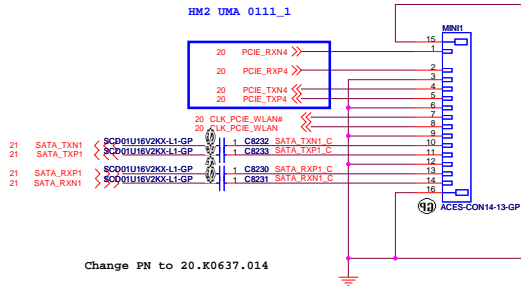
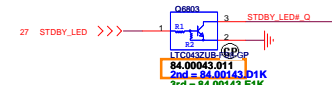


## HM2-CR -1 0220 by EDWIN for EMI request

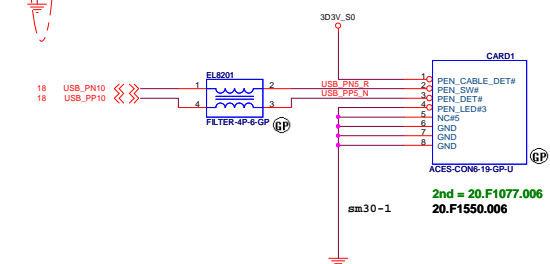
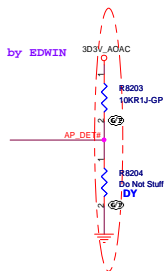
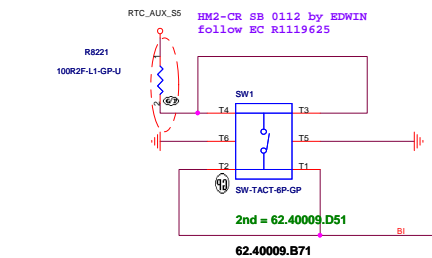
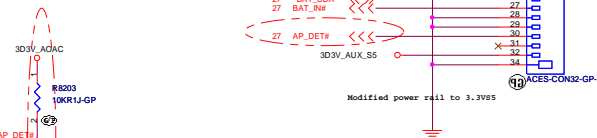
## Battery LED1(CHARGE)



## Power STDBY\_LED



## HM2-CR SB 0118 by EDWIN

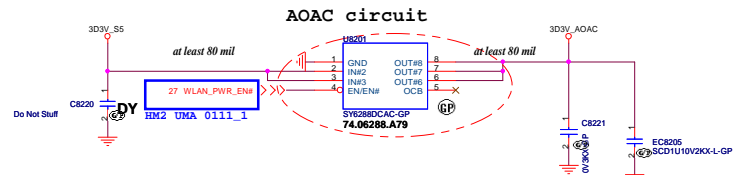


## HM2-CR SB 0118 by EDWIN

## Change solution as SM30

## HM2-CR -1 0206 by EDWIN

## Remove 2nd source



## Implement the battery reset function



5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

Elpida 1333 4G DS3 NonSSD 65W		
緯創資通		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
GPU Memory(2/5)		
Size	Document Number	Rev
Custom	HMA40 HR	-SA
Date: Tuesday, February 21, 2012	Sheet 84 of 102	





Elpida 1333 4G DS3 NonSSD 65W

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Title			
<b>GPU DPPWR/GND(5/5)</b>			
Size	Document Number		Rev
A3	<b>HMA40 HR</b>		<b>-SA</b>
Date:	Tuesday, February 21, 2012	Sheet 87 of	102

Elpida 1333 4G DS3 NonSSD 65W

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TitleGPU-VRAM1,2 (1/4)		
Size Custom	Document NumberHMA40 HR	Rev-SA
Date: Tuesday, February 21, 2012	Sheet 88	of 102



5

4

3

2

1

D

D

C

C

B

B

A

A

Elpida 1333 4G DS3 NonSSD 65W

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Title		
GPU-VRAM3,4 (2/4)		
Size	Document Number	Rev
Custom	HMA40 HR	-SA
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Title		
GPU-VRAM5,6 (3/4)		
Size	Document Number	Rev
Custom	HMA40 HR	-SA
Date:	Tuesday, February 21, 2012	Sheet 90 of 102

Elpida 1333 4G DS3 NonSSD 65W

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM7,8 (4/4)			
Size	Document Number		Rev
Custom	HMA40 HR		-SA
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Eplida 1333 4G DS3 NonSSD 65W		
緯創資通 <b>Wistron Corporation</b> <small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,            Taipei Hsien 221, Taiwan, R.O.C.</small>		
Title		
<b>RT8208B +VGA CORE</b>		
Size	Document Number	Rev
Custom	<b>HMA40 HR</b>	<b>-SA</b>
Date: Tuesday, February 21, 2012	Sheet 92 of	102

# Blanking

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Title <div>DISCRETE VGA POWER</div>		
Size <div>A4</div>	Document Number <div>SM30 HS</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>93</div> of <div>102</div>

LVDS Channel A

Blanking

Elpida 1333 4G DS3 NonSSD 65W

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
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Title

**LVDS Switch**

Size  
A4

Document Number

**SM30 HS**

Rev  
**-SA**

Date: Tuesday, February 21, 2012

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Title <div>CRT Switch</div>		
Size <div>A4</div>	Document Number <div>SM30 HS</div>	Rev <div>-SA</div>
Date <div>Tuesday, February 21, 2012</div>		Sheet <div>95</div> of <div>102</div>

SSID = SDIO

# Blanking

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Elpida 1333 4G DS3 NonSSD 65W

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**TOUCH PANEL**

Size  
A4

Document Number

**SM30 HS**

Rev

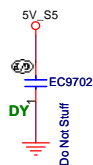
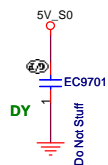
**-SA**

Date: Tuesday, February 21, 2012

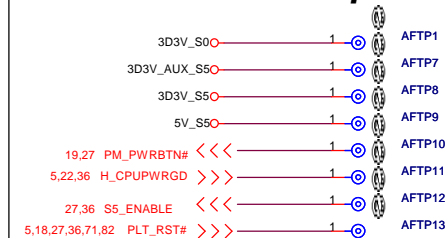
Sheet 96 of 102



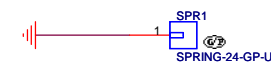
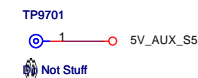
HM2-CR SB 0117 by EDWIN  
request by EMI



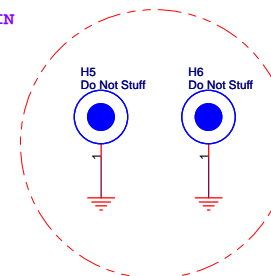
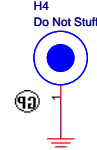
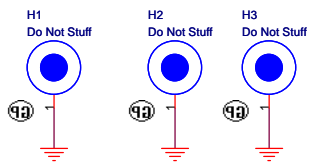
## Check test point



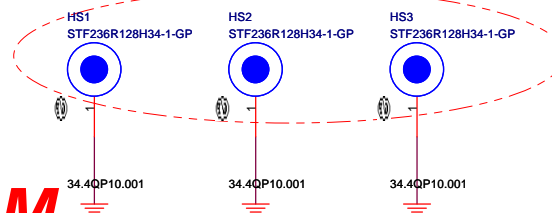
Test Point放在Dimm Door打開可量測處



HM2-CR SB 0112 by EDWIN  
update symbol



HM2-CR -1 0220 by EDWIN  
Part Number change



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Title		
UNUSED PARTS/EMI Capacitors		
Size	Document Number	Rev
A3	HMA40 HR	-SA
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- (1) change U6001 to socket 62.10089.001
- (2) change SW\_L1 and SW\_R1 PN to 『62.40089.221』
- (3) KI.G6501.001 / IC BD82HM65 SLH9D MM#908753 B2 FCBGA 989  
KI.G6501.004 / IC BD82HM65 SLJ4P MM#914377 B3 FCBGA989P
- (4)U3101 change PN to 71.08158.M02
- (5)DM2 1st -> change PN to 62.10024.G01
- (6) IMIC1 =>82.40012.001
- (7) RJ1 =>22.10177.J71
- (8) CPU1 =>1st change PN to 62.10055.321
- (9) USB2 =>1st change PN to22.10218.G01 -> only Lab stage

[Lab] S01G ==>1st  
S02G ==>2nd(NEC Cap)

Coin Battery:  
1st:23.20068.001  
2nd:23.22063.001

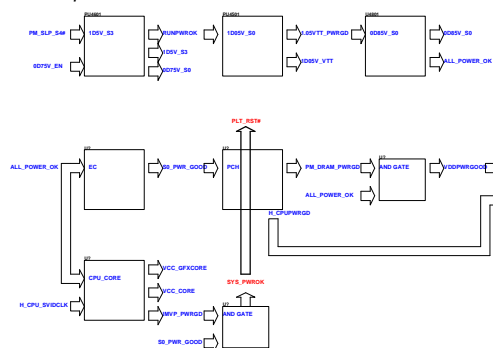
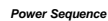
-SA

-SB

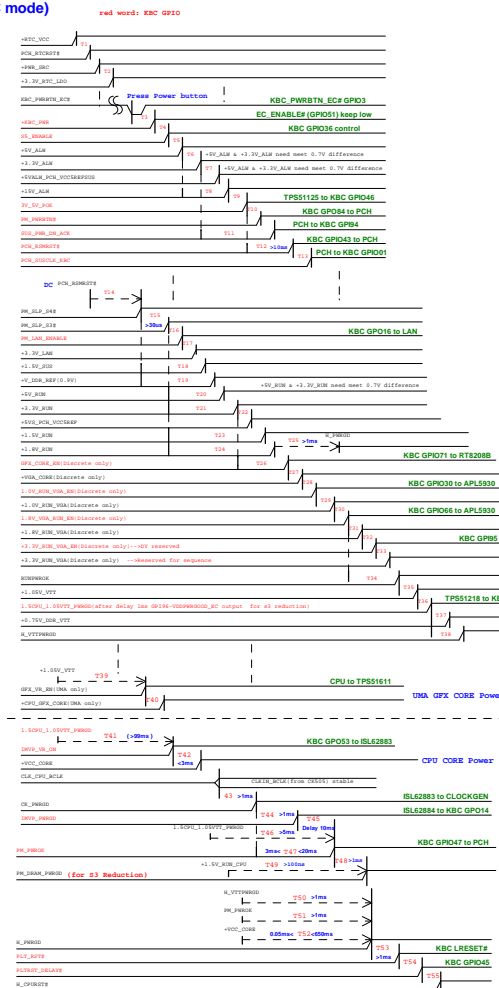
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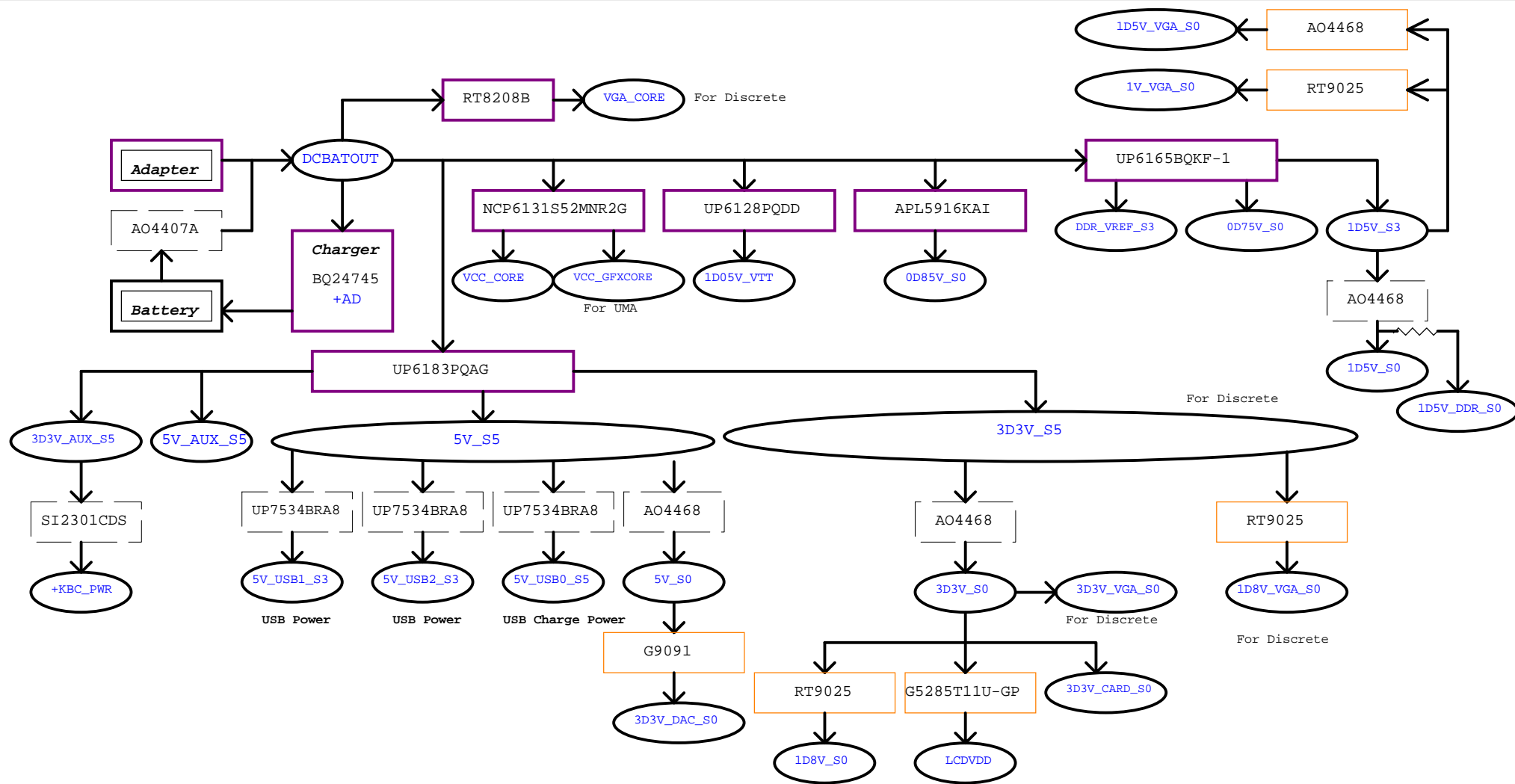
-2

(AC mode)



(DC mode)

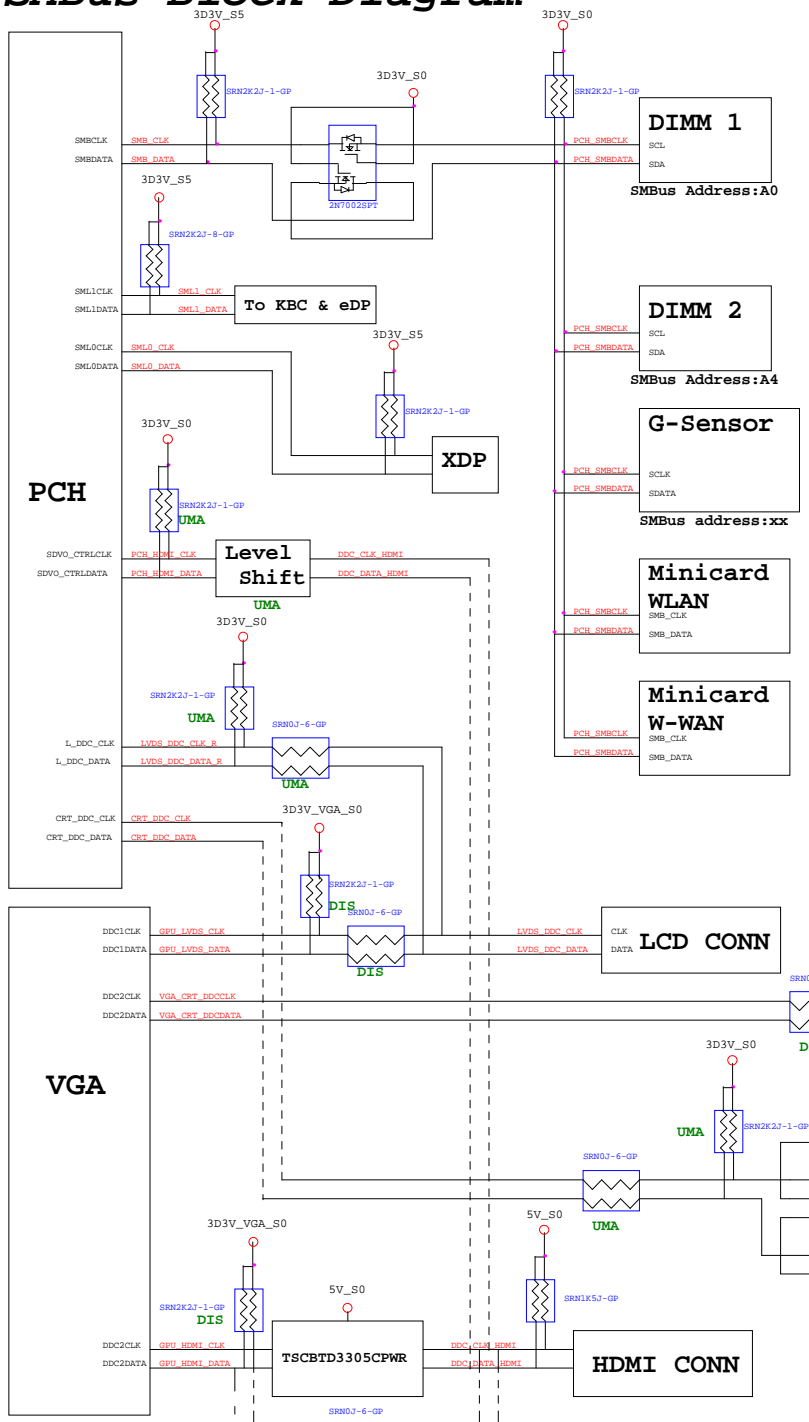




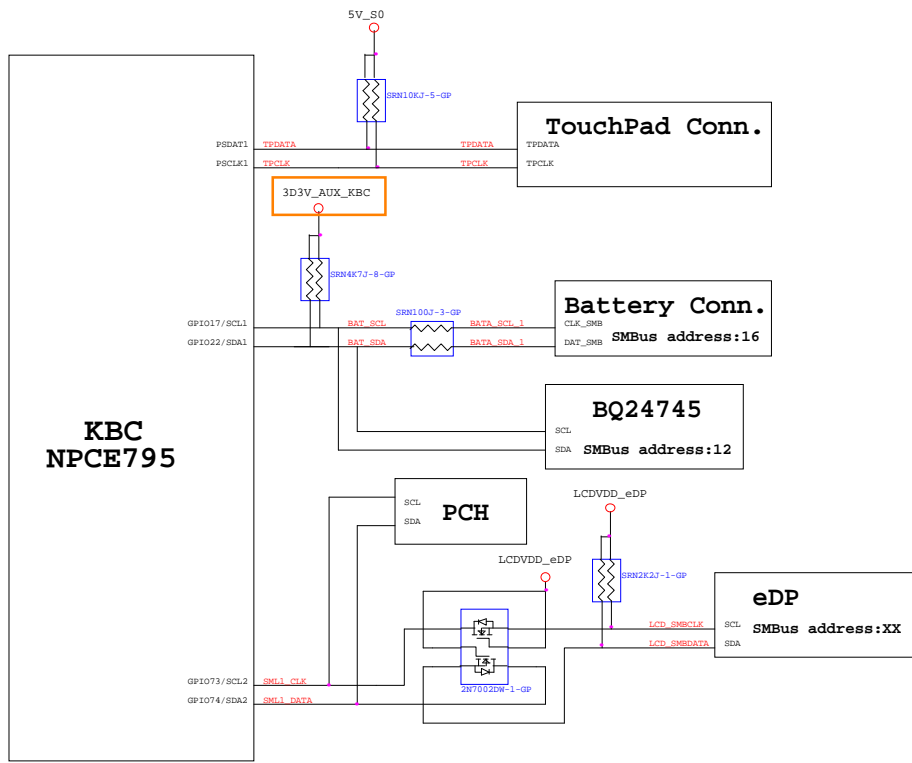
**Power Shape**



PCH SMBus Block Diagram

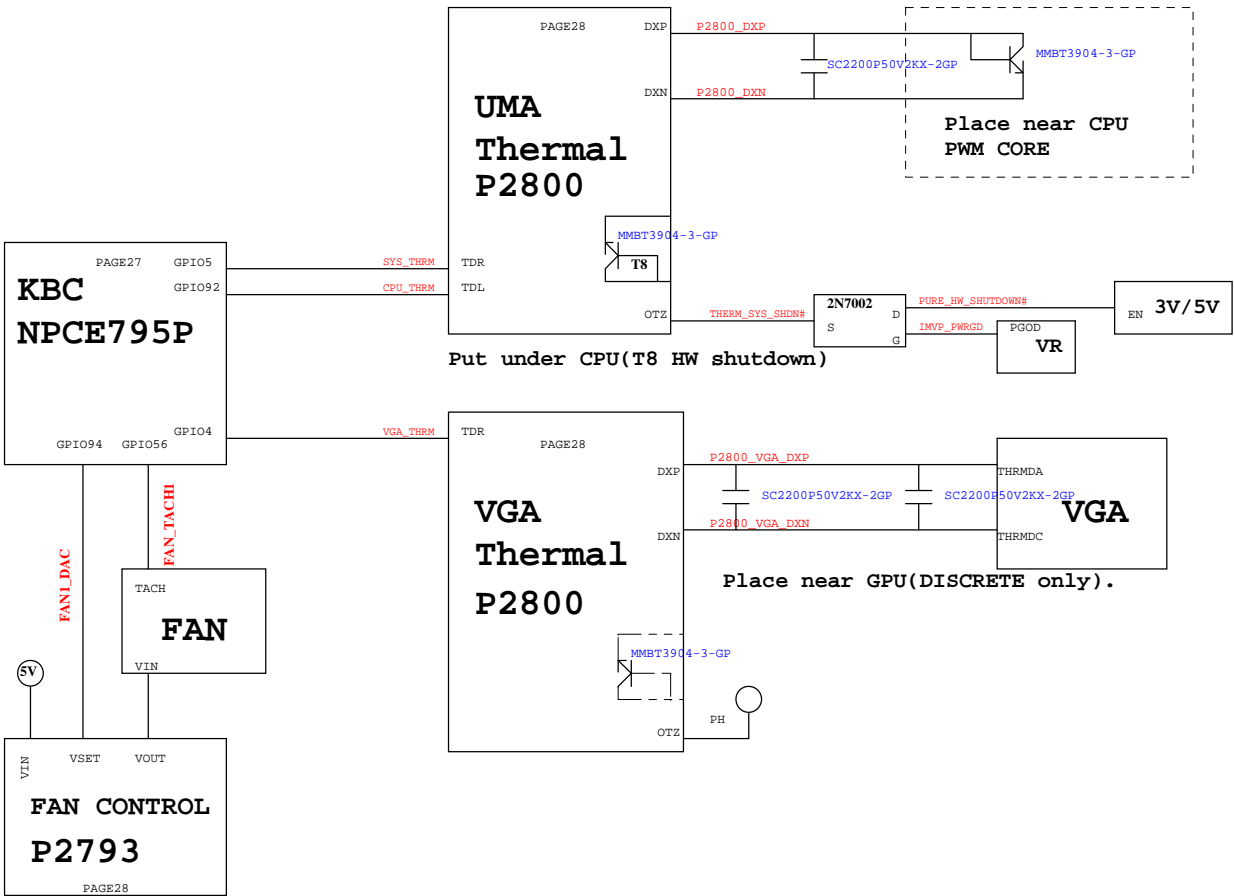


KBC SMBus Block Diagram



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# Thermal Block Diagram



# Audio Block Diagram

